Real Time Reconfigurability for UWB Receiver

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Abstract—Real time reconfigurability of the digital backend of UWB receiver has a potential to achieve significant power saving during the acquisition and synchronisation mode of receiver operation. This paper proposes a novel real time reconfigurability algorithm which can estimate number of parallel blocks required for the receiver operation for a particular channel condition and switches off the unwanted blocks. As a part of the real time reconfigurability algorithm, modified CLEAN and priority encoder algorithms are proposed for estimation and effective translation algorithms are developed in order to achieve significant reduction in receiver backend power consumption.

Index Terms— Adaptive control, Adaptive signal processing, Intelligent systems, Reconfigurable architectures

I. INTRODUCTION

Wireless sensor networks (WSNs) is one of areas in which, Ultra Wideband (UWB) technology can be used as a communication module. Communication, location tracking and ranging capabilities of UWB and possible low power digital implementation make it a potential candidate to be employed in WSNs. Some of the application areas of WSNs are health care, safety and security systems, agriculture, aviation, logistics and transportation.

UWB impulse radio is one of the most suitable technologies for WSN applications. It has been standardised for low to medium data rate applications under IEEE 802.15.4a for wireless personal area networks (WPAN) and WSNs[1]. Impulse radio is carrierless communication which uses short duration pulses of the order of few hundreds of pico-seconds (ps) to a few nano-seconds (ns) to transmit the data using different pulse modulation schemes [2].

The mostly digital transceiver architecture designed for <960MHz UWB band of operation performs coherent detection using digital domain pulse correlation. At the transmitter the data is coded using a pseudo-noise (PN) sequence and the pulse train is modulated using binary antipodal modulation. The receiver consists of a low noise amplifier and a bank of parallel time interleaved analog to digital converters (ADC) to provide an effective sampling rate of 2GHz. ADC resolution for UWB can vary from 4 bit to 1bit [3]. The receiver performs three major operations acquisition and synchronisation (AS), tracking and data detection. It employs a bank of pulse matched filters (PMF) and pseudo-noise (PN) correlators for AS operation followed by tracking and data detection. In order to speed up AS operation and facilitate receiver operation in worst case channel condition, 128 PMFs and 11 x 128 PN correlators operate in parallel. Although the parallelism achieves its aims and reduces operating frequency, it results in very high power consumption in the AS mode as compared to the other modes [4-8].

A UWB receiver is typically designed to cope with the worst case channel condition and time delay; however, they are not worst at all times. The channel impulse and time delay change with time, environment and transmitter-receiver distance [8, 9]. The parallelism requirement analysis performed to find out the number of parallel blocks actually required for AS operation in different channel impulses and time delays concludes that

- Number of PMF’s and PN correlators required for processing the received signal for different channel impulses are different.
- For the same channel impulses if time delay increases the PMF required for AS operation increases significantly
- In very few channel impulse cases and higher time delay values all the 128 parallel PMF’s and successive PN correlators are required for operation.

The analysis identifies that time delay is the factor which decides the required number of parallel PMFs and successive PN correlators [8].

This paper presents a novel real time reconfigurability algorithm for the digital backend of the UWB radio receiver. This reconfigurability algorithm estimates the time delay and channel condition from the received signal during the first few pulses in AS mode. It then translates this information into number of parallel block required for AS mode operation and subsequently switches off the unwanted blocks. A parallelism requirement analysis showed that significant power saving in the AS mode can be achieved when reconﬁgurability is applied. The paper also proposes estimation and translation methods and presents their detailed design, results and analysis for 4bit, 2bit and 1bit input quantisation.

II. REAL TIME RECONFIGURABILITY ALGORITHM

The proposed novel real time reconfigurability algorithm consists of estimation, translation and control blocks. Figure 1 presents the block diagram of the UWB receiver and the real time reconfigurability algorithm. Estimation block extracts the information about channel impulse and time delay from the received signal. Translation block then translates this information to the number of parallel PMFs and successive PN correlators required for AS operation for the current channel condition. The control block then subsequently generates
enable/disable signals to switch off the unwanted blocks in order to save power.

In order to save power for majority of the AS mode, the estimation and translation operations have to be performed during the first few received pulses. The second important design constraint on the reconfigurability algorithm is to maintain the data detection error rate as compared to the normal receiver. Lastly the additional hardware to the normal receiver should be minimal to justify the power saved.

III. ESTIMATION ALGORITHM

UWB transmit signal undergoes multiple reflections from various objects, called multipaths, when it propagates through the channel. Time delay in the received pulse with respect to the transmit pulse is also observed. Equation (1) represents the generalised channel response.

\[ h(t) = \sum_{l=1}^{L} a_l \delta(t - t_l) \]

(1)

Where \( a_l \) is attenuation, \( t_l \) is time delay, \( L \) is number of multipaths. The channel impulse and time delay change with respect to time and environment of operation [8, 9]. A pulse train with pulses of width 3ns and pulse repetition period (PRP) of 128ns are used for transmission. The channel delay spread for indoor UWB channel varies from 20-60ns [8]. Therefore, a pulse along with all multipaths is assumed to have significant energy for a window of 64ns. Depending on the time delay this window can lie anywhere within the pulse repetition period of 128ns.

For this reason some sort of channel impulse and time delay estimation needs to be performed in order to obtain the location of the window of significant energy received within the pulse repetition period. Traditional, complex channel estimation algorithms would not serve the purpose in this case as they are aimed at bit error rate improvements and require very high sampling rates, additional pilot symbols and perform channel estimation over the entire preamble. Also, majority of them are implemented for offline processing where signal quantisation is not an issue. However, in our case received signal is quantised for 4bit, 2it or 1bit resolution. This is one of the challenges for real time reconfigurability algorithm.

For estimation block design we propose to estimate the location of the last significant energy sample number within the pulse repetition period of the first received pulse. This information can be used to estimate the PMF capturing the maximum energy.

The received signal \( [r(t)] \) is the convolution of transmitted signal \( [s(t)] \) and channel response \( [h(t)] \). In order to extract last significant sample number, we propose to perform deconvolution. CLEAN, which is an iterative algorithm, is one of the most popular deconvolution techniques used for channel modeling. A transmit pulse is passed through a channel and received signal is processed offline using CLEAN algorithm to extract channel tap. Successive iterations of CLEAN algorithm provide different channel taps [10].

Implementing the complex and iterative CLEAN algorithm for estimation is not justifiable for the preset aim. In addition to that, limited ADC resolution of 4bit, 2bit or 1bit is one of the challenges for estimation by CLEAN algorithm. Therefore, in this paper a simplified CLEAN algorithm, which is named as “modified CLEAN” is proposed for estimation. Simplification of CLEAN algorithm and limited input resolution may limit the accuracy of the estimates, however, in our case accuracy is relaxed since only the last significant number needs to be estimated and not exact channel attenuation values. Also, iterative nature of the CLEAN algorithm is reduced to a single operation which reduces hardware complexity and processing time. Figure 2 presents the flowchart for modified CLEAN algorithm processing in which LSS represents last significant sample number.

A pulse template, resembling transmitted pulse is used. Cross correlation is a simple filter with template samples as its coefficients. A 10\% threshold relative to the correlation peak ensures 90\% energy capture. The modified CLEAN algorithm works very efficiently for input resolution of 2bit and 4bit.

For 1-bit input resolution, received signal samples are a 256-bit long vector array of 0’s and 1’s which act as input data for the digital backend. Each bit in this vector array represents one sample in the received pulse. The last significant sample number estimation becomes as simple as determining the last sample which is ‘1’ within the 256-bit long pulse sample vector. In this paper a priority encoder algorithm is proposed for estimation for 1bit input resolution. The algorithm will take the 256-bit vector as input and outputs 8-bit wide last significant sample number.

In order to validate the estimation methods, un-quantised received signal pulses for 100 different channel impulses are obtained and last significant sample number is determined for each case by observing sample amplitudes with a 10\% threshold. Subsequently, these received signals are quantised by 4bit , 2bit and 1bit ADCs and the last significant sample number is estimated for each case by using the modified CLEAN algorithm for 4bit and 2bit quantisation and priority encoder algorithm for 1bit quantisation. Figure 3 presents the last significant sample number which is determined for no quantisation case and that determined by the modified CLEAN for 4bit and 2bit quantisation. Figure 4 presents the
same with priority encoder for 1bit quantisation.

It can be seen from Figure 3 that the last significant sample number estimation by modified CLEAN algorithm for 4-bit and 2-bit input quantisation closely resembles to that of actual channel for same threshold value. Quantisation error and extra cross correlation output samples result in the difference in last significant sample values for some channel impulses. This difference and number of cases slightly increase for LSS determination by priority encoder method as shown in Figure 4. This is primarily due to quantisation error; however, a linear trend line is close to the expected result. These differences can be easily compensated for in the translation block. These results and analysis provide a firm evidence of the efficiency and effectiveness of proposed estimation algorithms. The modified CLEAN and priority encoder can be implemented with least hardware addition in the current receiver due to their simplicity of operation. Also estimation is performed in the first received pulse and power can be saved for the remaining AS mode which meets all design constraints set for the real time reconfigurability algorithm.

IV. TRANSLATION ALGORITHM

Translation involves translating the last significant sample information from the estimation block into number of parallel PMFs and successive PN correlators required for AS operation. For an effective translation, the number of PMFs estimated by real time reconfigurability algorithm \( T_{pmf} \) should be equal to or greater than the PMF reported to capture the maximum energy in a normal receiver \( \text{pmf}_\text{ref} \), for same channel condition and time delay. If \( T_{pmf} < \text{pmf}_\text{ref} \), then the translation method is said to have failed since it can cause an error in data detection. However, the probability of data detection error depends on the closeness of \( T_{pmf} \) to \( \text{pmf}_\text{ref} \), due to the energy capture principle.

To develop the translation algorithm, it is assumed that the last significant sample lies in the centre of the PMF capturing maximum energy. This ensures that the translated number of PMFs actually covers the part of the pulse repetition period where significant energy is received. The proposed translation method 1 (TM1) is defined by equation (2)

\[
\begin{align*}
\text{if } \text{LSS} \leq 64 \text{ then } T_{pmf} &= \text{LSS}/2; \\
\text{if } \text{LSS} \leq 191 \text{ then } T_{pmf} &= \text{LSS} - 64; \\
\text{else } T_{pmf} &= 128 \\
\end{align*}
\]

In order to validate the translation method, \( \text{pmf}_\text{ref} \) values for a normal receiver are determined for 100 different channel impulses and time delay varying from 0-50ns. Later, for each of these channel impulses and time delays, estimation is performed using modified CLEAN algorithm for 4bit and 2bit quantisation and priority encoder for 1bit quantisation. Translation is performed using the translation methods. Percentage of failure cases, the figure of merit used to validate the translation methods is the percentage of channel impulses in which \( T_{pmf} < \text{pmf}_\text{ref} \). Figure 5 presents the percentage failures cases for the proposed translation methods.

It can be seen from Figure 5 that TM 1 works very well with almost 0% failure cases for all time delays for 4bit quantisation. It performs well for 2bit quantisation as well with less than 15% failure cases for time delays till 30ns and 0% for higher time delays. It is observed in individual simulation results that \( T_{pmf} \) value is very close to \( \text{pmf}_\text{ref} \) providing a low probability of data detection error.

For 1bit quantisation case TM1 results in approximately 50% failure cases for most time delay values. Similar to 2bit quantisation case individual simulations show that \( T_{pmf} \) values are very close to \( \text{pmf}_\text{ref} \) reducing probability of data detection error. Nevertheless, such a high percentage of failure cases for lower time delay values from 0-30ns, may
lead to high data detection errors, as significant energy within the pulse repetition may not be captured due to low value of $T_{\text{pmf}}$. For higher time delay values, this does not have such an effect due to higher values for $T_{\text{pmf}}$.

In order to reduce the percentage of failure cases for lower time delay values in TM 1, the proposed TM 2 uses a guard band of 32 PMFs and is defined in equation (3)

$$\begin{align*}
\text{if } T_{\text{pmf}}_1 \leq 32; \text{ then } T_{\text{pmf}}_2 &= T_{\text{pmf}}_1 + 32; \\
\text{else } T_{\text{pmf}}_2 &= T_{\text{pmf}}_1
\end{align*}$$

With the guard band, the percentage failure cases are reduced for lower values of time delays, as seen in Figure 5. Average relative power saving percentage after reconfiguration is estimated assuming that 100% power is consumed when all 128 PMFs are ‘on’ and is presented in Figure 6. A significant amount of power saving can be achieved for different quantisation and time delays. For a typical time delay of 30ns in the indoor environment the reconfigurability can achieve a power saving of more than 10% for 4bit and 2bit quantisation and approximately 50% for 1bit quantisation.

Data detection was performed by transmitting and receiving sample data bits over different channel conditions in the simulation environment for normal and reconfigurable receiver to compare the data detection error rate. The results show that the proposed estimation and translation methods maintain the same data detection error for 4bit and 2bit quantisation cases. For 1bit quantisation the reconfigurability performs better than receiver without reconfigurability with 0.5% reduction in the detection error for time delay values of 0-20ns, a marginal increase of 0.6% in detection errors for time delays of 30-40ns and same detection error for remaining time delays. The small increase in data detection error for certain cases can be easily compensated in the error detection and correction block of the receiver.

The proposed translation methods are simple, thus hardware implementation is small, fast and consumes low power. Once translation is done the control block generates enable/disable signals to switch off the unwanted PMFs and PNCs.

V. CONCLUSION

In this paper a novel real time reconfigurability algorithm is proposed to reduce power consumption in the digital backend of a UWB receiver during the acquisition and synchronisation mode. Proposed modified CLEAN algorithm is used for estimation of channel condition for 4bit and 2bit and priority encoder algorithm is used for 1bit quantisation. Simple and effective translation methods are proposed to determine parallelism required. Simulation results indicate that the estimation and translation methods are very effective in power saving and achieve all the design constraints set for the real time reconfigurability algorithm.

REFERENCES