A HIGHLY EFFICIENT RECONFIGURABLE ARCHITECTURE FOR AN UTRA-TDD MOBILE STATION RECEIVER

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ABSTRACT

A novel reconfigurable architecture has been proposed for a mobile terminal receiver that can reduce power dissipation dependant on adjacent channel interference. The proposed design can automatically scale the number of filter coefficients and word length respectively by monitoring the in-band and out-of-band powers. The new architecture performance was evaluated in a simulation UTRA-TDD environment because of the large near far problem caused by adjacent channel interference from adjacent mobiles and base stations.

The UTRA-TDD downlink mode was examined statistically and results show that the reconfigurable architectures can save a maximum of 75% to 90% power dissipation respectively when compared to a fixed filter length of 57 and ADC word length of 16 bits. This will prolong talk and standby time in a mobile terminal. The average number of taps and bits were calculated to be 15 and 10 respectively, for an outage of 97%.

1. INTRODUCTION

This paper proposes a novel low-power reconfigurable architecture for a mobile terminal receiver. The architecture consists of a digital filter with a variable filter length and a variable word length pipelined analog-to-digital converter (ADC). The filter length and word length depend on the amount of interference experienced at certain times. When adjacent channel interference (ACI) is low, the required number of filter coefficients (taps) and word length (bits) are reduced which leads to lower power consumption. This is desirable in battery-powered terminals to increase talk and standby times. This reconfigurable system can be applied to various mobile standards by altering the tap values and the controlling code for the filter and ADC.

A UMTS terrestrial radio access (UTRA) system was chosen to demonstrate the power saving capabilities of this architecture. UMTS includes two duplex modes, frequency division duplex (FDD) and time division duplex (TDD). Figure 1 presents the two UTRA modes. In UTRA-FDD, the uplink and downlink transmissions use two separated radio frequency bands. In UTRA-TDD, uplink and downlink transmissions are carried over same radio frequency by using synchronised time intervals. Time slots in the physical channel are divided into transmission and reception part. Information on uplink and downlink are transmitted reciprocally [1].

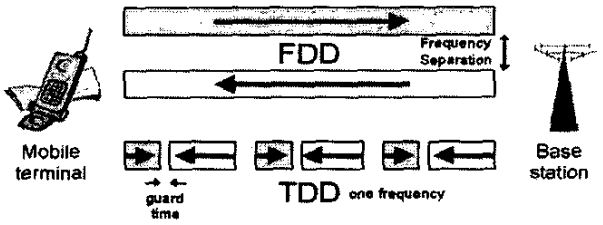

Figure 1. UTRA-TDD and UTRA-FDD modes

This makes TDD mode susceptible to ACI as nearby mobile stations (MS) and base stations (BS) cause interference to each other depending on frame synchronisation and channel asymmetry. This paper presents results for downlink UTRA-TDD operation due to its near far problem. Two interference sources exist in the downlink: adjacent MS and adjacent BS. The interference overlaps are BS→MS and MS→MS. If adjacent operators have synchronised frames and employ the same asymmetry, it would eliminate MS→MS interference [2]. This cannot be assumed in practice and hence interference is experienced from both sources dependant on frame synchronisation and asymmetry.

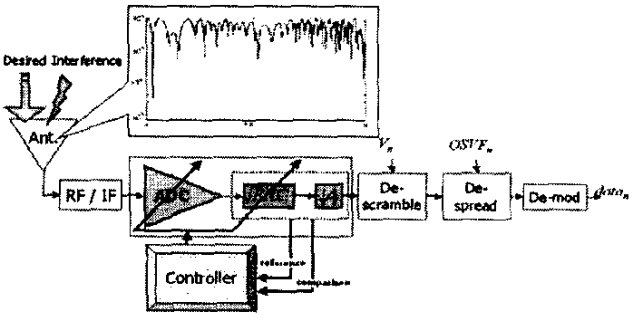

Figure 2. UTRA-TDD Mobile Station Receiver Block Diagram [3]

Figure 2 illustrates the architecture of an UTRA-TDD MS receiver. The block diagram demonstrates the general operation of the receiver showing the location of the proposed reconfigurable devices in the topology. A controller is proposed that makes a comparison between in-band (reference) and out-of-band (comparison) powers and scales the tap length and bit length of the filter and ADC.

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2. DOWNLINK INTERFERENCE ANALYSIS

This section of the paper looks at downlink analysis of ACI and derives mathematical models for filter and word lengths. UTRA-TDD downlink mode was examined in a simulation environment statistically with respect to ACI to obtain a cumulative distribution function (CDF) of filter lengths [4]. A CDF of word lengths is also found. The signal-to-noise ratio for the UTRA-TDD receiver is similar to that it [4] and is defined as:

$$Eb/No = \frac{Prx^i pg}{Prx^i(M-1) + I_{ad}{}^i + \eta + Q_n{}^i} \quad (1)$$

where Prx^i is the received desired signal power at the i^{th} MS in the cell of interest (COI). Processing gain is defined as pg. $Prx^i(M-1)$ is intra-cell interference where M is the number of users in the COI. $I_{ad}{}^i$ is the ACI received after applying a certain adjacent channel protection (ACP) factor. The ACP is the desired dB stop-band filter level in the adjacent channel. $I_{ad}{}^i$ is defined as:

$$I_{ad}{}^i = \frac{I_{total}}{ACP^i} \quad (2)$$

$Q_n{}^i$ is any left over noise in the system and is defined as the quantisation noise:

$$Q_n{}^i = G_k \bullet I_{ad}{}^i \quad (3)$$

where G_k is a gain control factor balancing $Q_n{}^i$ and ACP^i. If G_k is set to zero, the ACP^i will be at a minimum, therefore leaving no margin of error for $Q_n{}^i$.

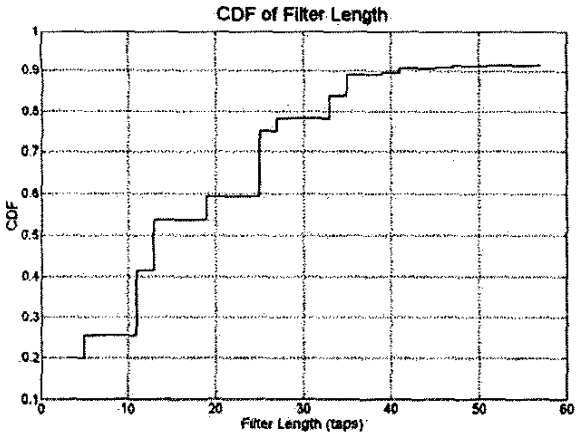

Figure 3. CDF of number of taps required for the filter ($G_k = 8$)

ACP values were converted to taps. It is clear from Figure 3 that with only five taps we obtain cell coverage of twenty percent and with twelve taps, it is forty two percent. A G_k value of 8 offers a suitable ratio between ACP^i and $Q_n{}^i$.

Figure 4 illustrates the CDF of the ADC word length values. The Qn values were converted to bits. It is clear from this figure that there is a low probability of high word length used.

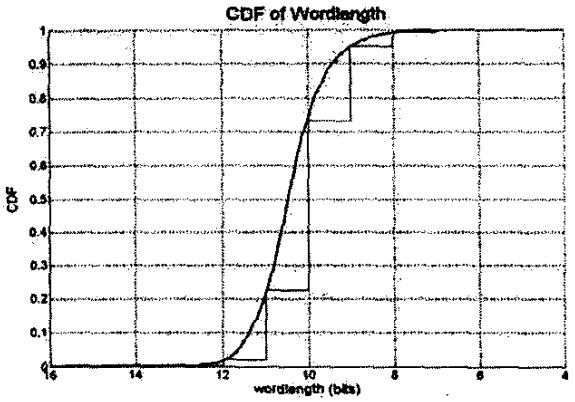

Figure 4. CDF of ADC word lengths ($G_k = 8$)

To determine the average number of taps and bits required, we perform the following calculations:

$$Average_{(taps/bits)} = \sum_{\zeta}^{n} \left(\frac{(Percentage(n) \bullet Length}{100} \right) \quad (4)$$

where *Percentage(n)* is the percentage of the time the filter or ADC has a length of n (calculating vertically from the CDF), *length* is the filter or ADC length. ζ corresponds to 3 for the filter and 1 for the ADC. Solving (4) yields average lengths of 15 and 10 for the filter and ADC respectively for an outage of 97%. The minimum number of taps is 5 and bits is 4. This was determined by inter symbol interference and quantisation noise analysis respectively.

3. PROPOSED RECONFIGURABLE ARCHITECTURE

This section of this document describes the proposed reconfigurable architecture in detail.

3.1 Digital Filter

The proposed filter is a pulse-shaping filter with a finite impulse response (FIR). The impulse response of the pulse-shaping filter is a root-raised cosine (RRC), $RC_0(t)$ given by [5]:

$$RC_0(t) = \frac{\sin\left(\pi \frac{t}{T_C}(1-\alpha)\right) + 4\alpha \frac{t}{T_C} \cos\left(\pi \frac{t}{T_C}(1+\alpha)\right)}{\pi \frac{t}{T_C}\left(1 - \left(4\alpha \frac{t}{T_C}\right)^2\right)} \quad (5)$$

where the roll-off factor $\alpha = 0.22$ and Tc is the chip duration of 2.6042e-7 seconds.

The system employs a folded FIR structure, and shaves off and adds taps to the ends of the impulse response to lower or raise the stop band dB level. The software/hardware partition of the filter architecture is presented in Figure 5. It consists of a DSP core and an application specific integrated circuit (ASIC). The DSP core is used for the intelligent controller, coefficient buffer and input sample buffer. The ASIC using standard digital libraries will consist of four multiply-accumulate (MAC) units, a LPHP block that outputs the desired low pass and unwanted high pass signals. The final components of the ASIC are the full wave rectifiers and the LPF networks. The operation of the DSP core and ASIC components in the reconfigurable digital filter architecture are as follows:

Coeff Buffer – This unit is the storage location of the filter coefficients. Only half the coefficients are stored along with the center coefficient as FIR filters exhibit symmetry. Internal pointers are used to keep track of which coefficients need to be processed. The *shaver* input adjusts a coefficient offset when more or less filter coefficients are needed.

Input Sample Circular Buffer – This component accepts the input samples *x(n)* and stores them in a circular buffer. This type of buffer structure reduces the amount of hardware switching which results in lower power dissipation. The *shaver* adjusts an input sample offset when there is a change in the amount coefficients needed. Input samples need to be summed before multiplication with coefficients due to the folded structure. This is demonstrated as follows:

$$out(i) = Input(n) + Input(K-n) \;\ldots\; 0 \geq n \geq \frac{K-1}{2} \qquad (6)$$

where *Input(n)* is the input sample at location *n* in the buffer and *K* is the filter length.

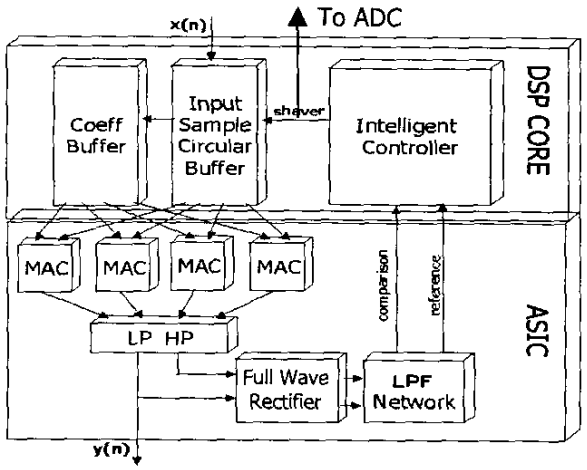

Figure 5. Reconfigurable Digital Filter Architecture

MAC units – There are four MAC units each performing a signed multiplication and accumulating the result in a register. As there are four MAC units, the filter structure is capable of shaving a maximum of eight taps per cycle.

LPHP unit – This component outputs the wanted (low pass) and interference (high pass) signals. The high pass signal is obtained by a simple subtraction operation. The output of the filter is subtracted from the input sample stored in the centre location of the input sample buffer.

Full Wave Rectifier – This component is a simple two's compliment algorithm. Both desired and interference signals are full wave rectified to obtain the absolute values.

LPF Network – This component is a low complexity digital infinite impulse response filter matching an analog signed order network. Clearly varying amplitudes are obtained from each signal.

Intelligent Controller – This is the brain of the reconfigurable architecture. This unit accepts two inputs (comparison and reference) and by performing an intelligent algorithm it will determine how many taps or bits are required to be shaved off or added on to ensure the Eb/No is met at all times. The changes take place for the next frame input to the filter. The feedback loop is performed every frame to ensure the minimum number of taps and bits are used.

3.2 Pipeline ADC

The reconfigurable ADC circuit employs a pipeline topology. The architecture is controlled and scaled through the system controller, as shown in Figure 2. Figure 6 shows the topology of the reconfigurable ADC.

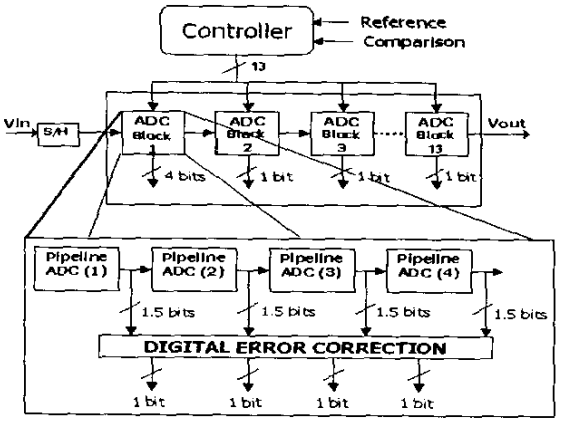

Figure 6. Reconfigurable Pipeline ADC System

The system employs thirteen pipeline blocks. The first block outputs 4 bits and the remaining twelve blocks output 1 bit each. Within each of these stages, a 1.5-bit pipeline topology is used, consisting of a sub-ADC, sub-DAC, a gain amplifier and a sample-and-hold (S/H) circuit. The sub-ADC used is a modified flash topology [6]. After analysing the different digital error correction (DEC) circuit architectures, the 1.5-bit/stage DEC scheme was found optimal for a low power, high throughput ADC. The overall system design and results of the DEC in this paper are based on a maximum 16-bit ADC.

4. POWER SAVING ANALYSIS

This section of this paper derives an estimate to the power that will be consumed by the novel reconfigurable architecture. The model is defined as:

$$P_{architecture} = P_{filter} + P_{ADC} \quad (7)$$

where P_{filter} is the dynamic power consumption of the filter:

$$P_{filter} = \left(\frac{n \bullet P_{MAC}}{2} + P_{MAC} \right) + P_{HPF} + P_{DSP} + P_{OTHER} \quad (8)$$

where n is the current filter order, P_{MAC}, P_{DSP} and P_{HPF} are the dynamic power consumptions a MAC unit, a DSP core proportional to the number of instructions and the high pass filter respectively. P_{OTHER} is defined as:

$$P_{OTHER} = P_{FULLRECT} + P_{LPF} \quad (9)$$

where $P_{FULLRECT}$ is the dynamic power consumption of two full wave rectifiers. This is minor as it is only a two's compliment operation. P_{LPF} consumes the approximate power of four multiplication operations (two filters).

P_{ADC} is the dynamic power consumption of the ADC:

$$P_{ADC} = \left(\frac{n}{\delta} \right) P_{BLOCK} + P_{DSP} + P_{S/H} + P_{DEC} \quad (10)$$

where n is the scalable word length, P_{BLOCK} is the dynamic power consumption of a specific ADC block of δ bits, P_{DSP} is the power dissipated by the DSP proportional to the number of instructions, $P_{S/H}$ is the power consumed by the front end S/H, and P_{DEC} is the power consumed by the digital error correction. Figure 7 illustrates the power analysis of the filter and ADC.

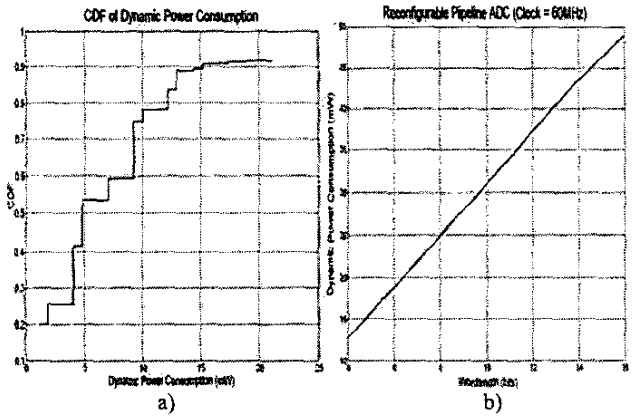

Figure 7. Power consumption analysis
a) Digital Filter b) Pipeline ADC

P_{filter} yields an average power consumption of (5.4mW + PDSP) using Alcatel 0.35micron CMOS with a clock of 20MHz. P_{ADC} consumes an average power of (31.22mW + PDSP) with a clock of 60MHz for the entire pipelined chain.

Solving (7) yields a total average power consumption of (36.62mW + P_{DSP}). The ADC can save a maximum of 75% power when 4 bits are required. The filter can save a maximum of 90% power when 5 taps are used. It must be stated that power consumption can drastically decrease with technology scaling. It must also be stated that the DSP core is not just used for the filter and ADC alone but for other components in the transceiver. Therefore, the area and power dissipation of the DSP will be shared.

5. CONCLUSION

A novel reconfigurable architecture was presented. The architecture consists of a digital filter and an ADC. The filter architecture utilises a DSP core and ASIC. It employs a folded FIR structure and automatically shaves off and adds taps to the ends of the impulse response. This is dependant on the in-band and out-of-band power ratios. This results in lowering or raising the stop band dB level. The ADC topology consists of a DSP intelligent controller and an ASIC. It employs a pipeline ADC, which could be scaled to different resolutions, depending on the ACI. If out-of-band powers are low, then the word length and filter lengths can be reduced resulting in large power savings.

In addition, power dissipation estimations were presented along with discussions. It can be said that this architecture will vastly reduce the power consumption compared to a fixed length filter structure and fixed word length ADC when large stop-band attenuations are not always required. A maximum of 75% to 90% power reduction is available for a 3G UTRA-TDD system. The reduction is likely to be higher for the FDD system because MS→MS ACI does not exist in this duplex mode.

6. REFERENCES

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