A Real-Time Reconfigurable Pipelined Architecture With Advanced Power Management For UTRA-FDD

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Abstract - **A reconfigurable-pipelined architecture with advanced power management has been proposed for a mobile terminal receiver that can reduce power dissipation. The design can automatically scale the number of filter coefficients and word length respectively by monitoring the in-band and out-of-band powers. The new architecture performance was evaluated in a simulation UTRA-FDD environment. A power consumption analysis of the implemented architecture is also presented.**

The UTRA-FDD downlink mode was examined statistically and results show that the reconfigurable architecture can save an average 70 percent power dissipation when compared to a fixed filter length of 41 and ADC word length of 16 bits. This will prolong talk and standby time in a mobile terminal. The average number of taps and bits were calculated to be 11 and 7 respectively.

I. INTRODUCTION

This paper describes a real-time reconfigurable architecture with advanced power management for a mobile terminal receiver. The architecture consists of a digital filter with a variable filter length pipelined to a variable word length pipeline analog-to-digital converter (ADC). The filter length and word length depend on in-band and out-of-band power ratios. When out-of-band power, referred to as adjacent channel interference (ACI), is low, the required number of filter coefficients (taps) and word length (bits) are reduced which leads to lower power consumption. This is desirable in battery-powered terminals to enhance talk and standby times. This reconfigurable system can be applied to various mobile standards by altering the tap values and the controlling code for the filter and ADC.

A UMTS terrestrial radio access (UTRA) system was chosen to demonstrate the power saving capabilities of this architecture. UMTS includes two duplex modes, frequency division duplex (FDD) and time division duplex (TDD). Figure 1 presents the two UTRA modes. In UTRA-FDD, the uplink and downlink transmissions use two separated radio frequency bands. In UTRA-TDD, uplink and downlink transmissions are carried over same radio frequency by using synchronised time intervals. Time slots in the physical channel are divided into transmission and reception part. Information on uplink and downlink are transmitted reciprocally [1, 2].

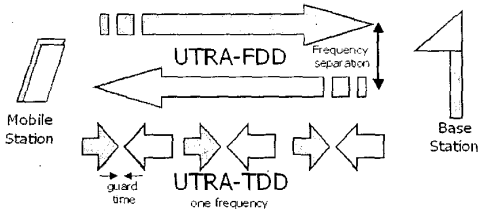

Figure 1. UTRA-TDD and UTRA-FDD modes

This paper presents results for downlink UTRA-FDD operation. One adjacent interference source exists in the downlink: base station (BS) to mobile station (MS). Figure 2 illustrates the architecture of an UTRA MS receiver. The block diagram demonstrates the general operation of the receiver showing the location of the reconfigurable devices in the topology. The control unit is the advanced power management device. It automatically, in real-time, calculates the most efficient filter length and word length of the filter and ADC respectively by monitoring in-band and out-of-band signal powers.

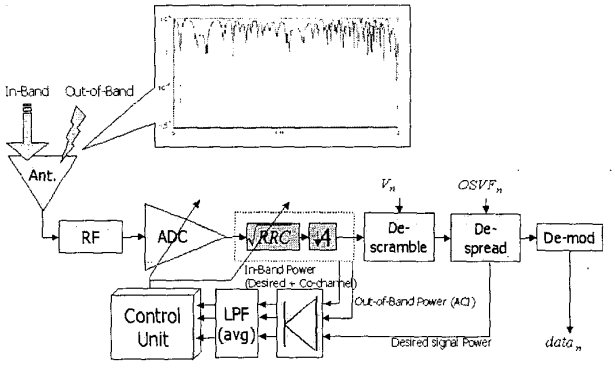

Figure 2. UTRA Mobile Station Receiver Block Diagram

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II. RECONFIGURABLE ARCHITECTURE

This section of this document describes the reconfigurable architecture in detail.

A. Digital Filter

The filter is a digital pulse-shaping low pass filter (LPF) with an impulse response $RC_0(t)$ given by [3]:

$$RC_0(t) = \frac{\sin\left(\pi \frac{t}{T_C}(1-\alpha)\right) + 4\alpha \frac{t}{T_C}\cos\left(\pi \frac{t}{T_C}(1+\alpha)\right)}{\pi \frac{t}{T_C}\left(1-\left(4\alpha \frac{t}{T_C}\right)^2\right)} \quad (1)$$

where the roll-off factor $\alpha = 0.22$ a bandwidth equal to the chip-rate of 3.84Mc/s. The chip duration is 1/chip-rate. The sampling frequency is 15.36MHz as the chip rate is over sampled by a factor of four. The channel filter architecture is presented in Figure 3. It consists of a direct form finite impulse response (FIR) structure where the output of the filter is a decimated convolution of the input and its coefficients.

The novel components that allow the filter to scale its filter length are a high-pass filter (subtraction operation) to obtain the out-of-band signal, three full-wave rectifiers, the three low pass filters to compute a running average and a control unit.

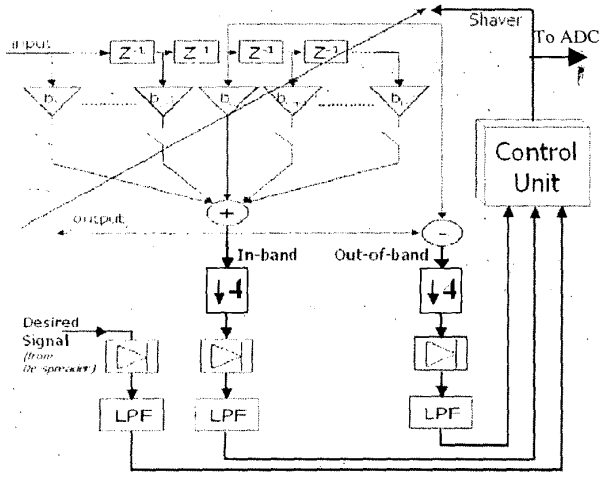

Figure 3. Reconfigurable Digital Filter System

The running average LPF's are not complex and have a first order infinite impulse response (IIR) where only two additions and two multiplications are required in hardware.

The output of the filter is the *in-band* signal (desired and co-channel) and the *desired* signal is obtained from de-spread component in the receiver. The control unit is the intelligence behind the architecture. It calculates the appropriate filter length based on the three signals by calculating the required ACS dB. The control unit then adjusts the filter length with the *shaver* signal. This signal adds or subtracts taps to the ends of the impulse response and is defined as:

$$shaver = \frac{Max_{flength} - New_{flength}}{2} \quad (2)$$

where $Max_{flength}$ is the maximum filter length available and $New_{flength}$ is the new calculated filter length. For example, if $New_{flength}$ is 19 and $Max_{flength}$ is 65, *shaver* is set to 23. Therefore, 23 taps from each end of the impulse response will be switched off and the other will be switched on. The minimum filter length was calculated to be 5 taps as in [4].

B. Pipeline ADC

The reconfigurable ADC circuit employs a pipeline topology. The architecture is controlled and scaled through the system control unit, as shown in Figure 2. Figure 4 shows the topology of the reconfigurable ADC.

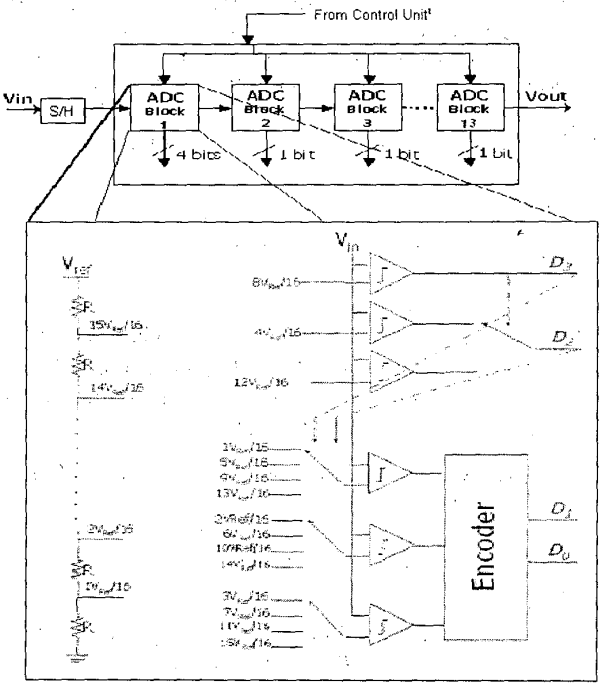

Figure 4. Reconfigurable Pipeline ADC System

The system employs thirteen pipeline blocks. The first block is a 4-bit subranging ADC similar to that in [5]. The minimum word length was calculated to be 4 bits [6]. The remaining twelve blocks output 1 bit each. Within each of the remaining 1-bit blocks, a 1.5-bit pipeline topology is used, consisting of a sub-ADC, sub-DAC, a gain amplifier and a sample-and-hold (S/H) circuit. After analysing the different digital error correction (DEC) circuit architectures, the 1.5-bit/stage DEC scheme was found optimal for a low power, high throughput ADC. The overall system design and results of the DEC in this paper are based on a maximum 16-bit ADC.

C. Control Unit Design

The control unit is the intelligence behind the architecture. It calculates the appropriate filter length and word length for the filter and ADC respectively. The equations for the control unit are derived from the signal to noise ratio similar to that in [4] and is as follows:

$$Eb/No = \frac{\Pr x^i pg}{\Pr x^i (M-1) + \frac{I_{total}{}^i}{ACP^i} + \eta + Q_e{}^i} \quad (3)$$

where Prx^i is the received desired signal power at the i^{th} MS in the cell of interest (COI). Processing gain is defined as pg. $Prx^i(M-1)$ is co-channel interference where M is the number of users in the COI. The adjacent channel protection (ACP) factor is defined by ACP^i. Thermal noise is given by η. $I_{total}{}^i$ is the ACI signal received. It is mathematically represented as:

$$I_{total}{}^i = \sum_{j=1}^{H} \frac{Ptx^j M^j}{\kappa^j{}_{B_m}} \quad (4)$$

where $\kappa^j{}_{B_m}$ is the path loss between the j^{th} adjacent channel BS causing interference and the mobile located at m in the COI. M^j is the number of users served by the j^{th} BS. Ptx^j is the j^{th} adjacent BS transmission power.

$Q_e{}^i$ is remaining noise in the system and is defined as the quantisation noise:

$$Q_e{}^i = G_k \bullet \frac{I_{total}{}^i}{ACP^i} \quad (5)$$

where G_k is a gain control factor balancing $Q_e{}^i$ and ACP^i. If G_k is set to zero, the ACP^i will be at a minimum, therefore leaving no margin of error for $Q_e{}^i$.

Substituting (5) into (3) and solving for ACP^i results in:

$$ACP^i = \frac{(Gk+1) I_{total}{}^i}{\left(1 + \frac{pg}{Eb/No}\right) \Pr x^i - \eta - \Pr x^i M} \quad (6)$$

where Prx^iM is the in-band signal. The actual attenuation of the filter is referred to as adjacent channel selectivity (ACS). The ACS depends on the Adjacent Channel Leakage Ratio (ACLR) as well as the ACP requirement. The ACLR is the ratio of the transmitted interference power to the power measured after a receiver filter in the +/-5MHz offset. The relationships have been investigated in [7] and it is found that:

$$ACS^i = \frac{1}{\frac{1}{ACP^i} - \frac{1}{ACLR}} \quad (7)$$

With the new calculated value for the ACP, the quantisation noise can be calculated in the control unit as in equation (5). Once $Q_e{}^i$ is solved, the word length of the ADC is calculated as follows:

$$Bits^i = \frac{10 \bullet \log 10\left(\frac{(I_{total}{}^i + \Pr x^i) \bullet Decimation_F}{Q_e{}^i}\right)}{6.02} + Safety_M \quad (8)$$

where $Decimation_F$ is the decimation factor used in the MS receiver, which is identical to the interpolation factor used in the BS transmitter. $Safety_M$ is a noise margin to combat any large input spikes or anomalies. A 2-bit (12.04dB) $Safety_M$ is used.

III. Results

The architecture was analysed in two ways. A statistical analysis was performed to determine the average lengths for the filter and ADC. A power consumption analysis is also presented to demonstrate the efficiency of the architecture.

A. Statistical Analysis

The simulation platform is similar to that in [4] was used. Users in the COI and adjacent channel cells were placed randomly using a uniform distribution. Monte Carlo simulations were then carried out to obtain the cumulative distribution function (CDF) of lengths for the filter and ADC.

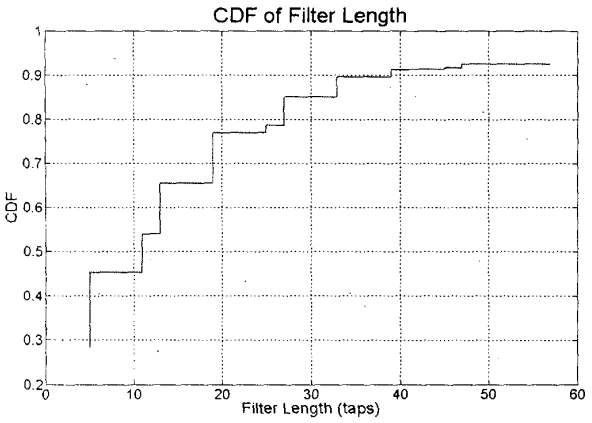

Figure 5. CDF filter length ($G_k = 8$)

The results obtained are for a near full load of eight users in each of the seven adjacent channel interfering cells and a near full load in the COI. A lognormal shadowing variable of 12dB was used in the simulation.

ACS values were converted to taps. It is clear from Figure 5 that there is a low probability of large filter lengths. The average filter length is 11. A G_k value of 8 offers a suitable ratio between ACP' and Q_e'. It Figure 6 illustrates the CDF of the ADC word length values. It is clear from this figure that there is a low probability of high word length used where the average word length is 7 bits.

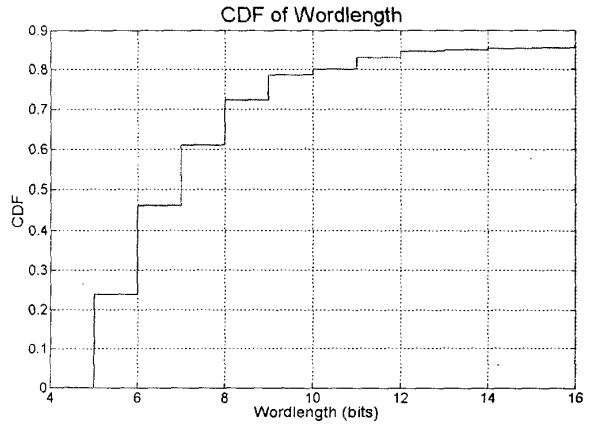

Figure 6. CDF of ADC word lengths ($G_k = 8$)

The average lengths for the filter and ADC are efficient compared to a filter and ADC with a length of 41 taps and 16 bits respectively. Average efficiency savings of 75 percent and 56 percent for the filter and ADC is available respectively in terms of taps and bits.

B. Power Consumption Analysis

This section demonstrates the power saving capabilities of the reconfigurable architecture. The total power consumed by the architecture is a summation of the dynamic power consumption of the filter and ADC as follows:

$$P_{architecture} = P_{filter} + P_{ADC} \tag{9}$$

The architecture was partitioned into application specific integrated circuit (ASIC) and digital signal processor (DSP). The control unit is implemented on a DSP as it exhibits flexibility while the other components in the architecture were implemented as an ASIC. An ASIC was chosen as it outperforms a DSP in terms of speed and power consumption. Figure 7 and 8 respectively illustrate the power analysis of the filter and ADC.

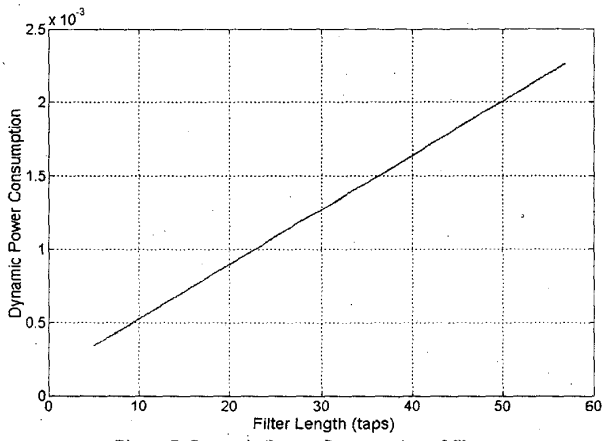

Figure 7. Dynamic Power Consumption of filter

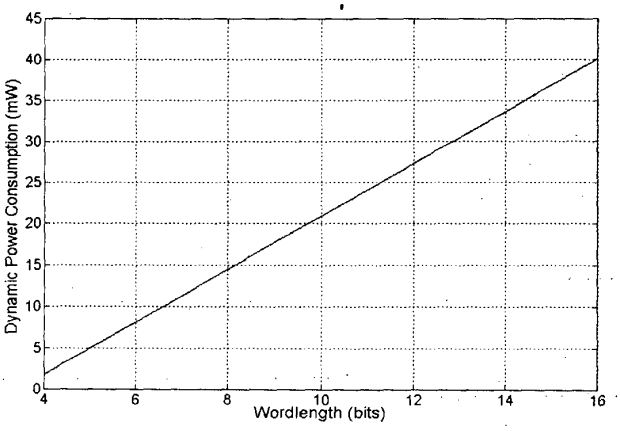

Figure 8. Dynamic Power Consumption of ADC

P_{filter} yields an average power consumption of (560uW excluding control unit) using Synopsys Design Ware libraries with a clock of 15.36MHz. P_{ADC} consumes average power of (12mW excluding control unit) with a clock of 15.36MHz.

Solving (9) yields a total average power consumption of (12.56mW excluding control unit) for the reconfigurable architecture. The average power savings for the reconfigurable architecture is 70 percent. It must be stated that power consumption can drastically decrease with technology scaling. It must also be stated that the DSP is not just used for the architecture alone but for other components in the transceiver. Therefore, the area and power dissipation of the DSP will be shared.

IV. Conclusion

A real-time reconfigurable architecture with advanced power management was presented. The architecture consists of a digital filter and an ADC. The filter architecture utilises a DSP core and ASIC. It employs a FIR structure and automatically shaves off and adds taps to the ends of the impulse response. This is dependant on in-band and out-of-band power ratios. This results in lowering or raising the stop band dB level. The ADC topology consists of a DSP intelligent controller and an ASIC. It employs a pipeline ADC, which could be scaled to different resolutions, also dependant on in-band and out-of-band power ratios. If out-of-band powers are low, then the word length and filter lengths can be reduced resulting in large power savings.

In addition, power dissipation savings were presented along with discussions. It can be said that this architecture will vastly reduce the power consumption compared to a fixed length filter structure and fixed word length ADC when large stop-band attenuations are not always required. An average power reduction of 70 percent is available for a 3G UTRA-FDD system.

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