IMPLEMENTATION OF A RECONFIGURABLE ARCHITECTURE

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ABSTRACT

Implementation of a reconfigurable architecture for an UTRA-TDD mobile terminal receiver is described. The architecture consists of a variable length digital channel filter and a variable word length pipeline ADC. The lengths depend on in-band and out-of-band power ratios. The architecture is power efficient and only consumes minimum power to meet the signal to noise ratio of the system. An average power consumption of 13.3 mW has been recorded.

1. INTRODUCTION

The need for communication is one of the prime necessities of people today. Wireless communications are advancing rapidly where major research is focused on new and innovated theoretical algorithm development and simulation. This will eventually lead to further enhanced communications and feature packed mobile devices where the main focus will be video streaming and Internet, not voice communication alone. Amid these high-tech feature packed mobile devices, a major bottleneck of cost will exist. The major cost factor in mobile devices is battery life. The more complex the device, the less the battery will last till it has to be charged, resulting in lower talk and standby times.

The reconfigurable architecture consists of a digital filter with a variable filter length and a variable word length pipelined analog to digital converter (ADC). The filter length and word length depend on in-band and out-of-band power ratios. When adjacent channel interference (ACI) and co-channel interference (CCI) is low, the required number of filter coefficients (taps) and word length (bits) are reduced which leads to lower power consumption. This is desirable in battery-powered terminals to increase talk and standby times. The downlink time division duplex (TDD) mode of UMTS terrestrial radio access (UTRA) was chosen due to its near far problem to demonstrate the power saving capabilities of this architecture.

Figure 1 presents the direct conversion UTRA-TDD mobile terminal receiver. The receiver is typical except for the addition of the reconfigurable components. The control unit accepts three signals (in-band, out-of-band and desired signal) with clearly varying amplitudes (obtained by the full wave rectifiers and running average filters). The controller now calculates the most efficient filter length and word length and reconfigures the filter and ADC respectively [1].

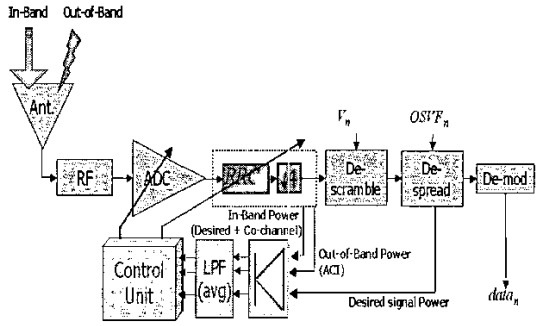

Figure 1. UTRA-TDD Mobile Receiver

2. RECONFIGURABLE ARCHITECTURE

The reconfigurable architecture is illustrated in Fig 3. The filter is a pulse-shaping filter with a finite impulse response (FIR). The impulse response of the pulse-shaping filter is a root-raised cosine (RRC), defined in [2]. The system employs a folded FIR structure, and shaves off and adds taps to the ends of the impulse response to lower or raise the stop band dB level [3]. The ADC circuit employs a pipeline topology [4].

The architecture is controlled and scaled through the system controller. The system employs thirteen pipeline blocks. The first block outputs 4 bits and the remaining twelve blocks output 1 bit each. A four bit modified flash sub-ADC [5] is used in the first pipeline block. The remaining twelve pipeline blocks use a 1.5-bit topology [6] consisting of a sub-ADC, sub digital to analog converter (DAC), a gain amplifier and a sample-and-hold (S/H) circuit.

3. IMPLEMENTATION

This section provides a description of the reconfigurable architecture implementation. The architecture was hardware software partitioned into application specific integrated circuit (ASIC) and digital signal processor

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(DSP). An ASIC was chosen for the power critical components due to its low power consuming and high-speed properties. A DSP was chosen for the control unit as it exhibits flexibility [7]. Only the ASIC implementation is presented of the reconfigurable architecture.

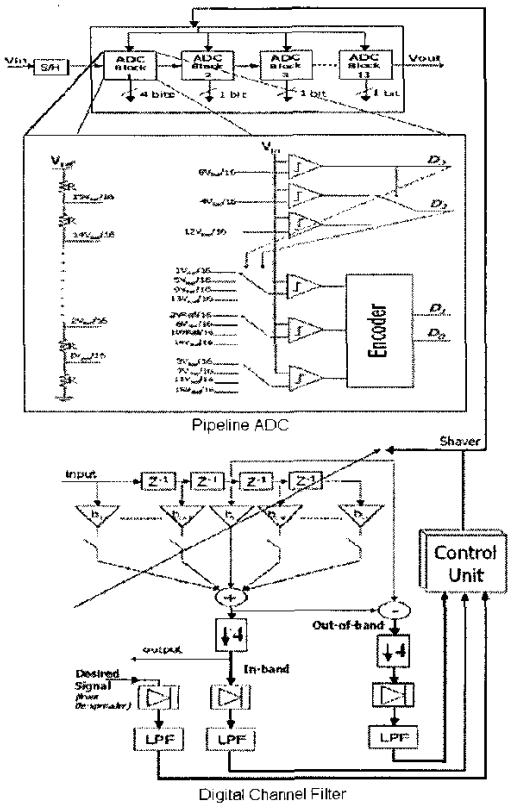

Figure 2. Reconfigurable Architecture

3.1. Semi-Custom Digital Filter

Figure 3 presents the top-level block diagram of the digital channel filter ASIC. A word-length of 16 bits is used for the *input* and 10 bits for *despread_in* (signal from de-spread block in receiver). The shaver signal is represented with 5 bits as this is ample for scaling the filter length. The *shaver* signal comes from the control unit. The output of the filter; *decimated_output* has a word length of 22 bits. The three inputs to the controller; *in_band, out_of_band* and *desired* also have word lengths of 22 bits. It is a synchronous system controlled by the *clk* and has an asynchronous *MR* (master reset). The *decimated_output* signal is processed every four clock cycles as the filter decimates by a factor of four. The *enable* signal initiates the filtering and *done* signals completion.

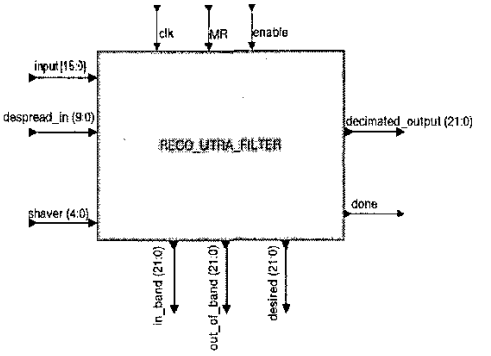

Figure 3. Block Diagram of Filter ASIC

The number representation in the system is signed 2's compliment fixed-point. Fixed-point numbers practically have the same precision as floating point numbers and have the advantage of lower power consumption in digital hardware. This is desirable for mathematical operations such as multiplications. Figure 4 presents a comparison of signed integer and signed fixed-point numbers.

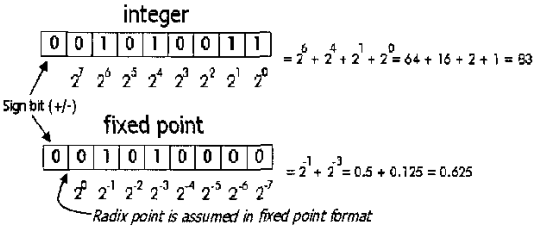

Figure 4. Signed integer vs. signed fixed-point numbers

The ASIC was hand coded in VHDL - register transfer language (RTL) and synthesized in Synopsys Design Compiler using DesignWare digital libraries.

3.2. Full-Custom Pipeline ADC

The pipeline ADC top-level block diagram is presented in figure 5.

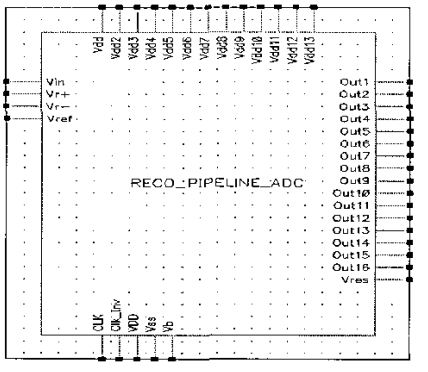

Figure 5. Block Diagram of ADC ASIC

The maximum resolution for the ADC is 16 bits where *Out1...Out16* are the digital output pins. *Vin* is the analog input to the ADC, *Vr+* and *Vr-* are the positive and negative reference voltages for the DAC, *Vref* is the input reference voltage, *CLK* and *Clk_Inv* are the clock and inverse clocks of the system, *VDD* and *Vss* are the supply and ground voltage respectively and *Vb* is the bias voltage. The control unit activates the pipeline blocks on or off through the *Vdd...Vdd13* pins. The residue output from the final pipeline stage is *Vres.*

The schematic of the ASIC was designed using the Analog Design Environment tool from Cadence and simulated using Spectre simulator. The layout of the ADC was performed on Layout Editor from Cadence using full custom libraries. Figure 6 illustrates the layout of the ADC.

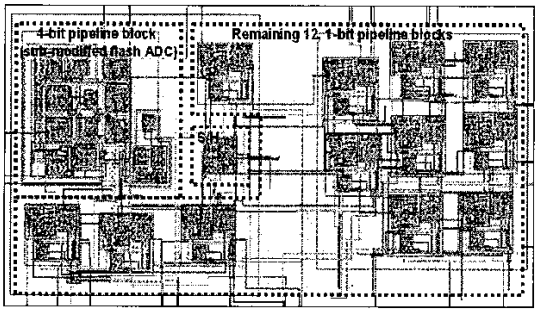

Figure 6. Layout of ADC ASIC

4. RESULTS

This section presents results of the implemented reconfigurable architecture. The filter and ADC results are first presented individually, and then a combined result of the architecture is presented.

4.1. Semi-Custom Digital Filter

A performance analysis was carried out on the filter ASIC to ensure it meets the timing requirement as well as low power requirements. The analysis was carried out in Synopsys Design Compiler. Table 1 presents the recorded attributes.

Table 1. Filter ASIC Results

Parameter	*Value*
Core Supply Voltage	1.62 V
Maximum Clock Frequency	22 MHz
Required Clock Frequency for UTRA-TDD	15.36MHz
Critical Path	45.11 nsec
Synthesis Libraries	Synopsys DesignWare
Core Area	N/A

The dominating factor in power consumption for a digital filter is the multiplier. Therefore, the power consumption should increase with a linear response as the filter length increases. Figure 7 presents a plot of the dynamic power consumption of the reconfigurable digital filter with respect to filter lengths. The results presented to not include the power of the control unit DSP (P_{DSP}), only the ASIC core.

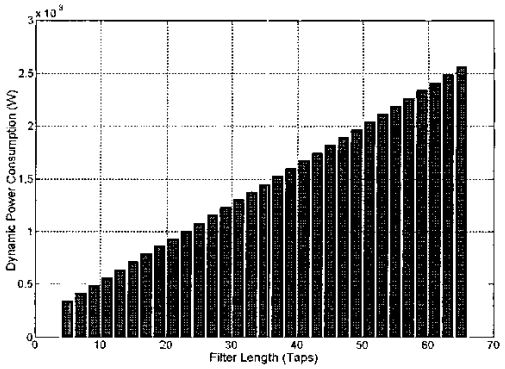

Figure 7. Dynamic Power Consumption of ASIC components in filter (clock = 15.36MHz)

It is clear from the above figure that as the filter length increases, the power consumption increases in a linear fashion. For a filter length of 5, the power consumption is 340μW excluding P_{DSP} and for a length of 65, it is 2.56mW excluding P_{DSP}.

4.2. Full-Custom Pipeline ADC

A performance analysis was completed on the ADC ASIC to ensure it meets timing requirements as well as low power properties. The analysis was carried out at layout stage. Table 2 presents the recorded results.

Table 2. ADC ASIC Results

Parameter	*Value*
Core Supply Voltage	2.5 V
Maximum Clock Frequency with 16 bits resolution	60 MHz
Required Clock Frequency for UTRA-TDD	15.36MHz
Critical Path	16.7 nsec
Layout Libraries	Full-Custom Cadence
INL	< 0.5 LSB
DNL	< 0.5 LSB
Core Area	0.35mm^2

Figure 8 illustrates the dynamic power consumption of the ADC. It is clear that as the word length increases, the power consumption increases proportionally. The power consumption ranges from 2.4mW to 40mW for word

lengths of 4 bits to 16 bits respectively. The results do not include P_{DSP}, only the ASIC core components.

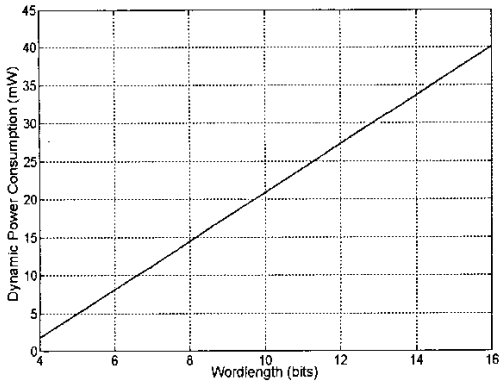

Figure 7. Dynamic Power Consumption of ASIC components in ADC (clock = 15.36MHz)

4.3. Architecture Performance Analsysis

The total power consumption the reconfigurable architecture consumes is a linear sum of the dynamic power consumption of the filter and ADC. Statistical showed that the average filter length is 15 and the average word length is 7. Therefore, the average power consumption of the reconfigurable architecture is 13.3mW excluding the power consumption of P_{DSP}

P_{DSP} will be proportional to the number of instructions for the control unit algorithm in a DSP core. If the feedback loop is performed every n samples, then the power consumption of the DSP core could be estimated as follows:

$$P_{DSP} = \frac{\#DSP\_Instructions}{n} \quad (1)$$

where *#DSP_Instructions* is the dynamic power consumption of the number of instructions in the DSP core. This will result in a minor power consumption increase.

5. CONCLUSION

This paper presented the implementation of a reconfigurable architecture for an UTRA-TDD mobile terminal receiver. The architecture consists of a variable length digital channel filter and a variable word length pipeline ADC. The length of the filter and ADC depend on in-band and out-of-band power ratios. The architecture is power efficient and only consumes minimum power to meet the signal to noise ratio of the system.

Analysis of the architecture took place at synthesis stage of the filter component, and layout of the ADC. An average power consumption of 13.3 mW has been recorded from the analysis of the reconfigurable architecture. This will increase talk time as well as stand by time of the mobile terminal.

This paper did not present the implementation and analysis of the control unit. The power consumed by the control unit will add a minor increase to the total power consumption of the architecture. The synthesis of the filter was performed with standard Synopsys Design Ware digital libraries and the results will vary when it is synthesized and floor planning is completed with a manufacturers technology file and libraries.

6. REFERENCES

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