DESIGN AND ASIC PERFORMANCE ANALYSIS OF A RECONFIGURABLE DIGITAL FILTER FOR A UMTS APPLICATION

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ABSTRACT

A reconfigurable digital root raised cosine (RRC) filter for a UMTS terrestrial radio access (UTRA) mobile terminal receiver is described and analysed. The filter monitors in-band and out-of-band received signal powers and calculates the appropriate filter length that meets the bit-energy to interference ratio (Eb/No). This design is advantageous, as only minimum battery power will be used resulting in power consumption savings compared to fixed filter length digital filters. A 70% average power reduction is available for the UTRA - time division duplex (TDD) system.

1 INTRODUCTION

The need for enhanced and efficient communication is one of the prime necessities of people today. Third generation (3G) wireless communications will offer wideband data and voice services that will enable applications such as wireless video conferencing and Internet. Amid these high-tech applications exists the major bottleneck of cost. The cost factor in this paper is the battery life in a mobile phone.

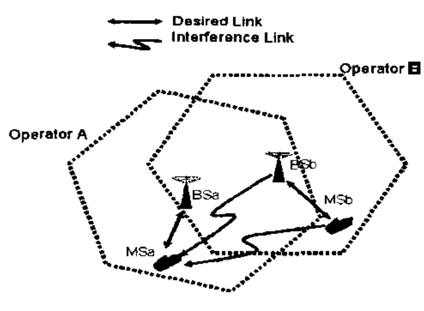

Figure 1. TDD Downlink interference scenario [2]

A reconfigurable digital RRC filter for an UTRA-TDD mobile receiver has been designed and analysed. UTRA-TDD has a near far problem where two interference sources exist in the downlink: adjacent mobile station (MS) and adjacent base station (BS). The interference overlaps are BS→MS and MS→MS [1,2]. This is illustrated in Figure 1. This reconfigurable filter only uses the required filter length to attenuate out-of-band adjacent channel interference (ACI) powers. When ACI and co-channel interference is low, there is no need for high adjacent channel selectivity (ACS) levels; therefore the filter length is reduced. This is desirable, as it will extend the battery life in the mobile. It is the opposite when ACI and co-channel interference are high. Figure 2 presents a frequency response of the filter with respect to in-band and out-of-band signals.

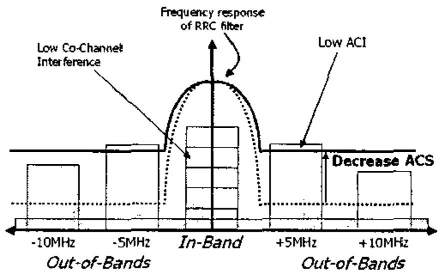

Figure 2. Spectrum with Reconfigurable Filter

2 FILTER DESIGN

This section of this document describes digital reconfigurable filter in detail. The filter is a pulse-shaping low pass filter (LPF) with an impulse response $RC_0(t)$ given by [3]:

$$RC_0(t) = \frac{\sin\left(\pi \frac{t}{T_C}(1-\alpha)\right) + 4\alpha \frac{t}{T_C}\cos\left(\pi \frac{t}{T_C}(1+\alpha)\right)}{\pi \frac{t}{T_C}\left(1-\left(4\alpha \frac{t}{T_C}\right)^2\right)} \qquad (1)$$

where the roll-off factor $\alpha = 0.22$ a bandwidth equal to the chip-rate of 3.84Mc/s. The chip duration is defined as:

$$Tc = \frac{1}{chiprate} = 0.2604\mu s \qquad (2)$$

The sampling frequency is 15.36MHz as the chip rate of 3.84 Mcps is over sampled by a factor of four. Figure 3 presents the frequency response with various filter lengths. The reconfigurable filter architecture is presented in

Figure 4. It consists of a direct form finite impulse response (FIR) structure where the output of the filter is a decimated convolution of the input and its coefficients. The novel components that allow the filter to scale its filter length are a high-pass filter (subtracter) to obtain the out-of-band signal, three full-wave rectifiers, the three low pass filters to compute a running average and a control unit.

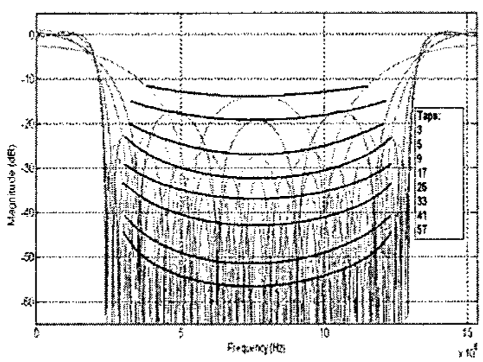

Figure 3. Frequency Response using various filter lengths

The output of the filter is the *in-band* signal (desired and co-channel) and the *desired* signal is obtained from de-spread component in the receiver.

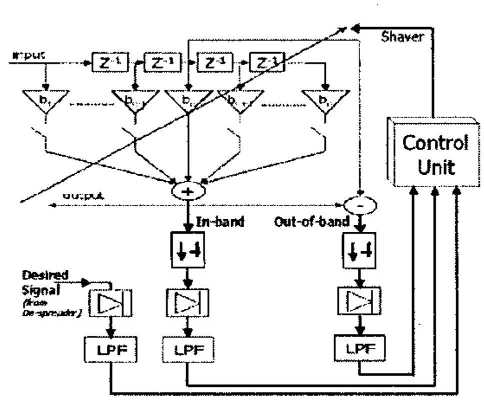

Figure 4. Scalable RRC Filter Block Diagram

2.1 High Pass Filter

This component is a subtraction operation in hardware. The *out-of-band* signal is obtained by subtracting a delayed input sample with the current output sample. A highly complex high pass filter (HPF) is not required.

2.2 Full Wave Rectifier

The three signals (*desired, in-band* and *out-of*-band) are prepared for the three running average LPF's by full wave rectifying them. Their amplitudes remain the same but are represented by their absolute value. The full-wave rectifiers are simple 2's compliment operations in digital hardware. If the signed bit of the word is logic 1, then the word is inverted and 1 is added. If it is logic 0, then the word is untouched.

2.3 Running Average Low Pass Filter

The three signals are averaged over a certain number of samples to obtain clearly varying amplitudes. The running average LPF's have a first order infinite impulse response (IIR). Two additions and two multiplications are required per filter. The output equation $y(n)$ is defined as follows:

$$y(n) = [(x(n) + x(n-1)) \bullet \alpha] + [y(n-1) \bullet \delta] \quad (3)$$

where $x(n)$ is the current input sample, $x(n-1)$ is a delayed input sample, $y(n-1)$ is a delayed output sample and α is defined as:

$$\alpha = \frac{(1-\delta)}{2} \quad (4)$$

δ is described as follows:

$$\delta = \frac{\cos\theta c}{1+\sin\theta c} \quad (5)$$

where θc is a normalised frequency of 0.002π.

2.4 Control Unit

The control unit is the intelligence behind the architecture. It calculates the appropriate filter length based on the three signals and adjusts the filter length by shaving off or adding taps to the ends of the impulse response. This lowers or raises the ACS dB level. The algorithm for the control unit is derived from the Eb/No equation below [4]:

$$Eb/No = \frac{Prx^i \bullet pg}{Prx^i(M-1) + I_{ad}^{\ i} + \eta} \quad (6)$$

where Prx^i is the received desired signal power at the i^{th} MS in the cell of interest (COI). Processing gain is defined as pg. $Prx^i(M-1)$ is co-channel interference where M is the number of users in the COI. Thermal noise is defined as η. $I_{ad}^{\ i}$ is the ACI received after applying a certain adjacent channel protection (ACP) factor. The ACP is a measure of overall system performance. It is the ratio of the total power transmitted from a source to the total interference power affecting a victim receiver. Solving (5) for ACP yields:

$$ACP^i = \frac{ACI^i}{\Pr x^i\left(1+\frac{pg}{Eb/No}\right) - \Pr x^i M - \eta} \quad (7)$$

where ACI^i is the *out-of-band* signal, Prx^i is the *desired* signal and Prx^iM is the *in-band* signal. The other variables are known and *Eb/No* is set at the target bit-energy to interference ratio. A look up table (LUT) in the controller converts the calculated ACP to the appropriate ACS, filter length and *shaver*. The relationship between the ACP and ACS is found in [5] and is:

$$ACS^i = \frac{1}{\dfrac{1}{ACP^i} - \dfrac{1}{ACLR}} \tag{8}$$

where the ACLR is the adjacent channel leakage ratio defined as the ratio of the transmitted power to the power measured after a receiver filter in the adjacent channel. The *shaver* signal switches on or off taps in the FIR structure. It is defined as:

$$shaver = \frac{Max_{flength} - New_{flength}}{2} \tag{9}$$

where $Max_{flength}$ is the maximum filter length available and $New_{flength}$ is the new calculated filter length. For example, if $New_{flength}$ is 19 and $Max_{flength}$ is 65, *shaver* is set to 23 (10111 in binary). Therefore, 23 taps from each end of the impulse response will be switched off and the other will be switched on.

2.5 Hardware Design

The filter architecture was hardware/software partitioned into digital signal processor (DSP) implementation for the control unit and semi-custom application specific integrated circuit (ASIC) for the other components. An ASIC was chosen for the power critical components due to its low power consuming and high-speed properties. A DSP was chosen for the control unit as it exhibits flexibility. The ASIC will be described here with its block diagram presented in Figure 5.

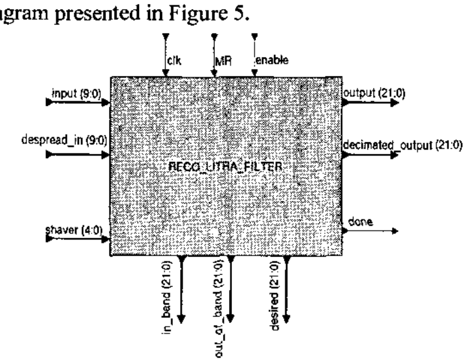

Figure 5. Block Diagram of ASIC

A word-length of 10 bits is used for the *input* and *despread_in* (signal from de-spread block in receiver). The *shaver* signal is represented with 5 bits as this is ample for scaling the filter length. The *shaver* signal comes from the control unit. The output of the filter; *decimated_output* and *output* have word lengths of 22 bits. The three inputs to the controller; *in_band, out_of_band* and *desired* also have word lengths of 22 bits. It is a synchronous system controlled by the *clk* and has an asynchronous *MR* (master reset). The *output* signal is processed in one clock cycle and the *decimated_output* signal every four clock cycles as it is decimated by a factor of four. The *enable* signal initiates the filtering and the *done* signals completion.

The number representation in the system is signed 2's compliment fixed-point. Fixed-point numbers practically have the same precision as floating point numbers and have the advantage of lower power consumption in digital hardware. This is desirable for mathematical operations such as multiplications. Figure 6 presents a comparison of signed integer and signed fixed-point numbers.

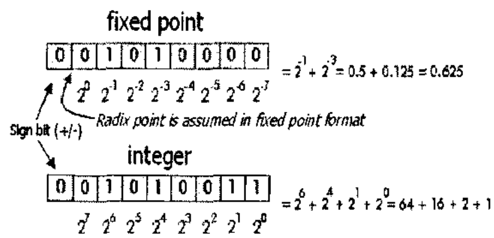

Figure 6. Signed integer vs. signed fixed-point numbers

The ASIC was hand coded in VHDL - register transfer language (RTL) and synthesized in Synopsys Design Compiler using DesignWare digital libraries.

3 RESULTS

3.1 Statistical Results

A statistical analysis in a simulation environment for the UTRA-TDD system was performed in [6] to determine the percentages of certain filter lengths. An average and minimum filter length was also found.

The analysis shows that there is a low probability of high filter lengths and a greater probability of lower filter lengths. This establishes that a reconfigurable filter of this type will be efficient as the majority of the time low filter lengths are required to attenuate out-of-band signals. The average filter length is 10.1. The minimum filter length was also found to ensure when low ACS levels are required; the quality of service (QoS) is still met. Inter-symbol interference was analysed and the minimum filter was recorded to be 5.

3.2 Hardware ASIC Results

The performance analysis was carried out on the ASIC to ensure it meets the timing requirement (sampling frequency of 15.36MHz) as well as low power requirements. The analysis was carried out in Synopsys

Design Compiler. Table 1 presents the recorded attributes of the ASIC.

Table 1. ASIC specifications

Parameter	Value
Core Supply Voltage	1.62 V
Maximum Clock Frequency	22 MHz
Critical Path	45.11 nsec
Synthesis Libraries	Synopsys DesignWare

The dominating factor in power consumption for a digital filter is the multiplier. Therefore, the power consumption should increase with a linear response as the filter length increases. Figure 7 presents a plot of the dynamic power consumption of the reconfigurable digital filter with respect to filter lengths. The results presented to not include the power of the control unit DSP (P_{DSP}), only the ASIC.

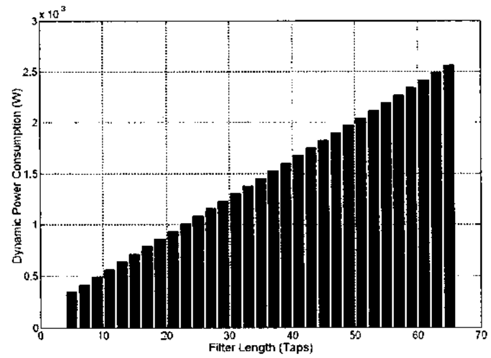

Figure 7. Dynamic Power Consumption of ASIC components (clk = 15.36MHz)

It is clear from the above figure that as the filter length increases, the power consumption increases in a linear fashion. For a filter length of 5, the power consumption is 340μW excluding P_{DSP} and for a length of 65, it is 2.56mW excluding P_{DSP}. Figure 8 illustrates a statistical analysis of the power consumption.

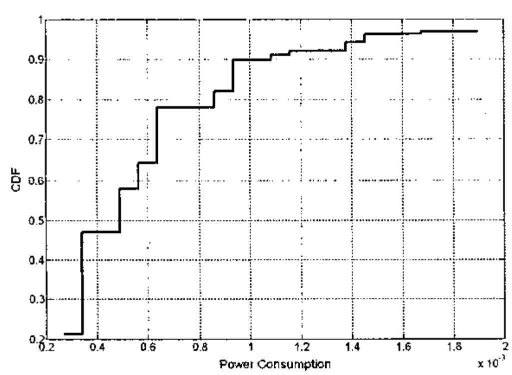

Figure 8. CDF of Dynamic Power Consumption of ASIC components (clk = 15.36MHz)

The statistical analysis shows that the filter on majority will consume low amounts of power. The average power consumption was calculated to be 564μW excluding P_{DSP}. P_{DSP} will be proportional to the number of instructions for the control algorithm in a DSP core. If the control loop is performed every n samples, then the power consumption of the DSP core could be estimated as follows:

$$P_{DSP} = \frac{P_{\#instructions}}{n} \quad (10)$$

This will result in a minor power consumption increase.

4 CONCLUSION

This paper has presented the design and performance analysis of a reconfigurable digital filter for an UTRA-TDD mobile terminal receiver. It was found that a fixed filter length is not power efficient, as high stop band levels are not always required. The average filter length was calculated to be 10.1 taps. This corresponds to an average power dissipation of 564μW excluding P_{DSP} and a 70% average power saving compared to a fixed filter length of 47 that meets the 3rd Generation Partnership Project specifications. The minimum filter length was found to be to 5 taps consuming 340μW excluding P_{DSP}.

This reconfigurable filter will be advantageous in next generation mobile phones, as it will prolong talk and standby times. This is desirable, as it will allow users to use multimedia services for extended periods before recharging batteries.

5 REFERENCES

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