CMOS ADC with Reconfigurable Properties for a Cellular Handset

A. Stojcevski, J. Singh, A. Zayegh

School of Electrical Engineering, Victoria University, Melbourne Australia
Email: Alex.Stojcevski@vu.edu.au

Abstract

A low power reconfigurable ADC architecture is described for a mobile terminal receiver. The architecture can automatically scale the resolution by monitoring in-band and out-of-band powers. The architecture performance was evaluated in a simulation UTRA-TDD environment. A power consumption analysis of the implemented architecture is also presented. The UTRA-TDD downlink mode was examined statistically and results show that the reconfigurable architecture can save an average of 74 percent power dissipation for TDD mode when compared to a fixed ADC word length of 16 bits. This will prolong talk and standby time in a mobile terminal.

1. Introduction

This paper describes a low power reconfigurable architecture for a mobile terminal receiver. The architecture consists of a variable word length pipeline analog-to-digital converter (ADC) and a control unit. The word length depends on in-band and out-of-band power ratios. When out-of-band power, referred to as adjacent channel interference (ACI), is low, the required word length (bits) is reduced which leads to lower power consumption. This is desirable in battery-powered terminals to enhance talk and standby times. This reconfigurable system can be applied to various mobile standards by altering the bit values and the controlling code for the ADC.

A UMTS terrestrial radio access (UTRA) system was chosen to demonstrate the power saving capabilities of this architecture. UMTS includes two duplex modes, frequency division duplex (FDD) and time division duplex (TDD). Figure 1 presents the two UTRA modes. In UTRA-FDD, the uplink and downlink transmissions use two separated radio frequency bands. In UTRA-TDD, uplink and downlink transmissions are carried over same radio frequency by using synchronised time intervals. Time slots in the physical channel are divided into transmission and reception part. Information on uplink and downlink are transmitted reciprocally [1,2]. This makes TDD mode susceptible to ACI as nearby mobile stations (MS) and base stations (BS) cause interference to each other depending on frame synchronisation and channel asymmetry.

The UTRA-TDD operation has a near far problem of receiving out-of-band signal powers from both adjacent mobile and base stations.

This paper presents results on the UTRA-TDD downlink operation. One adjacent interference source exists in the FDD downlink: base station (BS) to mobile station (MS). TDD downlink has two adjacent interference sources: BS→MS and MS→MS.

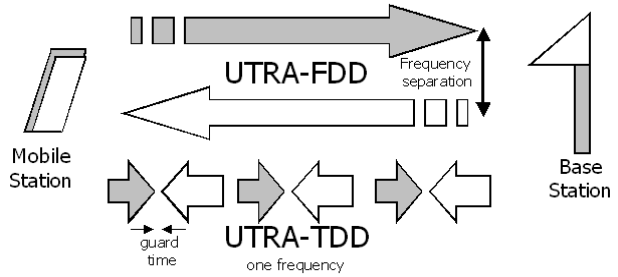

Figure 1: UTRA-TDD and UTRA-FDD modes [3]

Figure 2 illustrates the architecture of an UTRA MS receiver. The reconfigurable ADC architecture for a receiver is proposed in Figure 2. The architecture consists of pipeline ADC architecture, RRC filter, de-spreader, de-scrambler, de-modulator, decimation factor and signal power measurement.

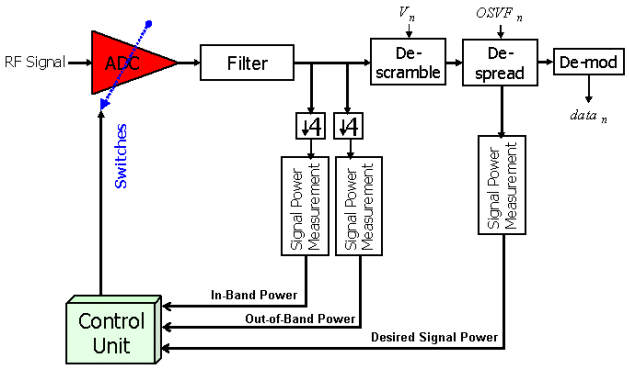

Figure 2. UTRA Mobile Station Receiver Block Diagram

Proceedings of the Second IEEE International Workshop on Electronic Design, Test and Applications (DELTA'04)
0-7695-2081-2/04 $ 20.00 © 2004 IEEE

2. Architecture Design

This section of the paper describes the reconfigurable architecture, similar to that in [4].

2.1 Pipeline ADC Design

The reconfigurable ADC circuit employs a pipeline topology. The architecture is controlled and scaled through the system controller, as shown in Figure 2. Figure 3 shows the topology of the reconfigurable ADC.

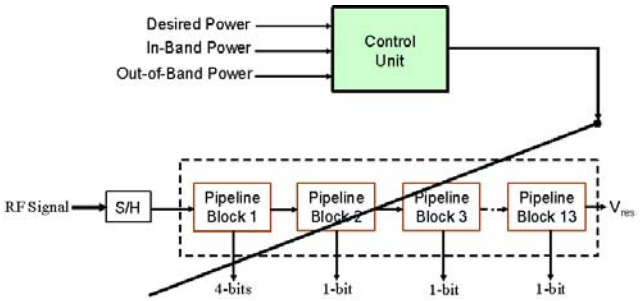

Figure 3. Reconfigurable Pipeline ADC System

The system employs thirteen pipeline blocks. The first block is a 4-bit modified flash ADC [5]. The minimum word length was calculated to be 4 bits [6]. The remaining twelve blocks output 1 bit each. Within each of the remaining 1-bit blocks, a 1.5-bit pipeline topology is used, consisting of a sub-ADC, sub-DAC, a gain amplifier and a sample-and-hold (S/H) circuit. After analysing the different digital error correction (DEC) circuit architectures, the 1.5-bit/stage DEC scheme was found optimal for a low power, high throughput ADC. The overall system design and results of the DEC in this paper are based on a maximum 16-bit ADC.

2.2 Control Unit Design

The three inputs required by the control unit in order to reconfigure the ADC, are obtained from the filter and the de-spreader. Clearly varying amplitudes of each signal is required before they are reprocessed by the control unit, where the most efficient Q_n is calculated. This is achieved by the signal power measurement components in the architecture where the signals are averaged over a certain length of time.

The controller is the intelligence behind the architecture. It calculates the appropriate filter length and word length for the filter and ADC respectively. The algorithm for the reconfigurable ADC is formulated from the *Eb/No* model given in Equation 1. Considering intra-cell interference is always present as orthogonality may not be achievable in practice and the received signal powers have been propagated.

$$Eb/No = \frac{\Pr x^i pg}{\Pr x^i (M-1) + \frac{ACI^i}{ACP} + \eta + Qn^i} \quad (1)$$

where $P_{rx}{}^i$ is the received desired signal power at the i^{th} MS in the COI and is defined as follows:

$$P_{rx}{}^i = \frac{P_{rec}{}^i}{\kappa^i} \quad (2)$$

$P_{rx}{}^i$ is determined by the code power of the BS divided by the path loss of the i^{th} MS within one time slot in the cell of interest (COI). The processing gain pg and thermal noise η are known (static), as well as the target bit energy to interference ratio (*Eb/No)*. Solving Equation 1 for $Q_n{}^i$ yields:

$$Q_n{}^i = \Pr x^i \left(1 + \frac{pg}{Eb/No}\right) - \Pr x^i M - \frac{ACI^i}{ACP} - \eta \quad (3)$$

2.3 Layout Implementation

The pipeline ADC top-level block diagram is presented in Figure 4. Partitioning is a critical aspect of layout implementation and must be considered very decisively.

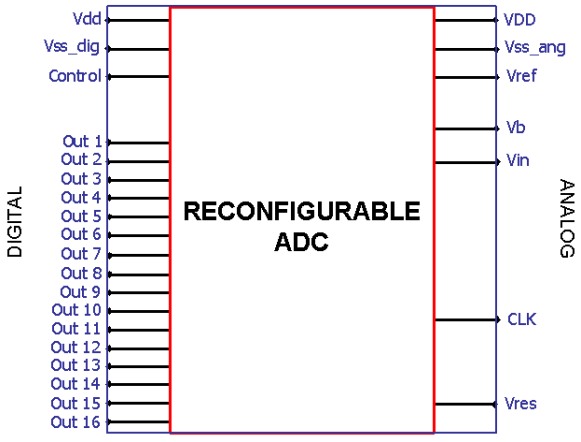

Figure 4. Block Diagram of ADC

The top level block diagram of the ADC shows all the digital inputs and outputs being at opposites sides as far

away from each other as possible. The maximum resolution for the ADC is 16 bits where *Out1…Out16* are the digital output pins. *Vin* is the analog input to the ADC, *Vref* is the input reference voltage, *CLK* is the clock of the system, *VDD* and *Vss_ang* are the power supply and ground to the analog section, respectively, *Vdd* and *Vss_dif* are the power supply and ground to the digital section respectively, *Vb* is the bias voltage, *Control* is the control signal that activates which and how many pipeline blocks need to be turn 'on', and *Vres* is the final analog output.

The schematic of the ADC was designed using the Analog Design Environment tool from Cadence and simulated using Spectre simulator. The layout of the ADC was performed on Layout Editor from Cadence using full custom 0.18µm technology. Figure 5 illustrates the layout of the 16-bits ADC. Once again the ADC layout shows the appropriate partitioning with the analog cells being separated from the digital cells. A guard ring around the analog section is also used.

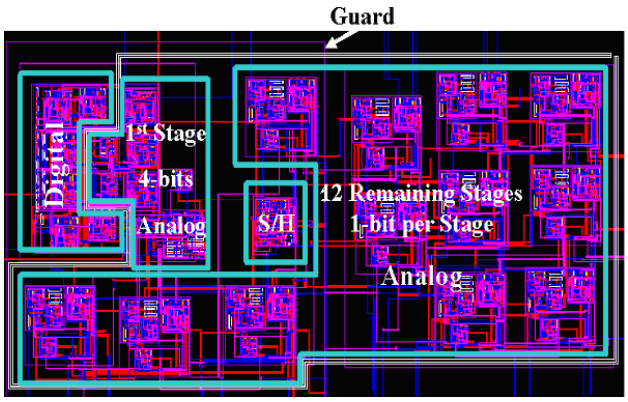

Figure 5. Layout of ADC

3. Results

3.1 Statistical Results

Users in the COI and adjacent channel cells were placed randomly using a uniform distribution. Monte Carlo simulations were carried out to obtain the cumulative distribution function (CDF) of the interference powers I_B and I_M, at each random point. In addition, the Q_n levels at each of these points were found. The results obtained are for a near full load of eight users in each of the seven adjacent channel interfering cells and a near full load in the COI. A lognormal shadowing variable of 12Db was used in the simulation obtained from the 3GPP specifications.

Figure 6 illustrates the CDF of the ADC word length values. Four different synchronisation factor (α) values were generated on each Monte Carlo run. Lognormal shadowing of 12Db was used. It is clear that there is a low percentage of higher Q_n and lower Q_n.

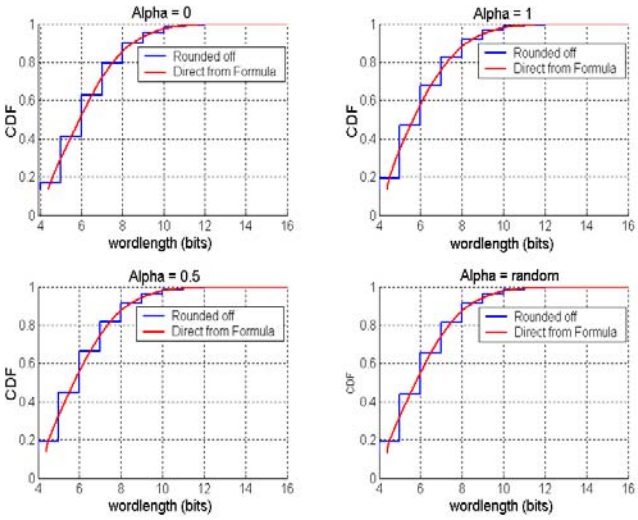

Figure 6. CDF of ADC word lengths

Table 1 provides a comparison of the different median and standard deviation values for all four different synchronisation factors.

Table 1. Effect on Resolution with different α.

Alpha	Median Value (bits)	Standard Deviation
α = 0	5.897	2
α = 1	5.649	2
α = 0.5	5.728	2
α = random	5.764	2

From Table 1 it can be summarised that even though the difference between the median values of the resolutions at different alpha values is significantly small, there is still some percentage of difference. In the implementation process the alpha values will not affect the resolution due to the rounding off condition. All resolution with decimal points will have to be rounded off to the higher resolution.

It can be observed in Table 1 that when the synchronisation factor α = 0, which means that there is MS → MS interference only, there is a high probability of the required resolution being between 3.897-bits and 7.897-bits.

When α = 1, meaning that there is only BS → MS interference, the probability of required resolution is slightly different to that when α = 0, and is between 3.649-bits and 7.649-bits. When α = 0.5, meaning that 50

% of the interference is from BS → MS and 50 % is from MS → BS, the probability of required resolution is between 3.728-bits and 7.728-bits. The final value for α = random, is when any possibility of interference can occur, and the probability of required resolution is between 3.764-bits and 7.764-bits.

All boundary values above are calculated using the standard deviation of 2. It can be seen that alpha has small affect on the resolution, therefore it can be stated that the highest probability of required resolution within the reconfigurable system is between 4 bits and 8 bits, and that resolution lower than 4-bits and higher than 10-bits will occur very rarely. Figure 7 illustrates CDF plots of the power consumption for the different synchronisation factors.

Once again a slight difference of power consumption for different alpha vales can be noticed. There has been a greater analysis performed on the plot of Figure 7 (d), due to the fact that here α is random, which what it would be in a real life scenario.

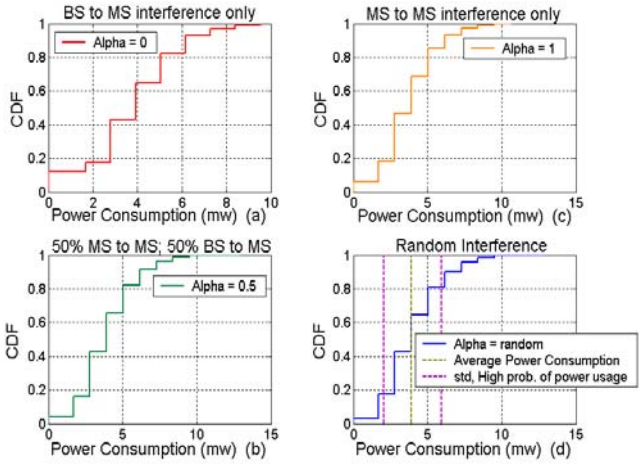

Figure 7. CDF of ADC Power Consumption

Figure 7 (d), shows the power consumption for the entire 16- bits ADC. The middle dotted line indicates the mean power consumption of the converter, which is 3.92Mw, and is present when the average 6-bits resolution of the reconfigurable ADC is used.

The other two dotted lines surrounding the mean power consumption dotted line, are the standard deviation boundaries, which indicate the highest probability of power usage of the reconfigurable architecture, which occur between 1.68Mw and 6.16Mw. These boundaries correspond to 4-bits and 8-bits.

The results of Figure 7 also justify the analysed results illustrated in Figure 6.

3.2 Implementation Results

A performance analysis was completed on the ASIC ADC to ensure it meets timing requirements as well as low power properties. The results are presented in Table 2.

Table 2. ADC Performance Results

Parameter	Performance Value
Core Supply Voltage	2.5 V
Maximum Clock Frequency with 16 bits resolution	60 MHz
Required Clock Frequency for UTRA-TDD	15.36MHz
Average Power Consumption @ 15.36 MHz	3.92 Mw
Average SNR	37.88 dB
Average DR	36.12 dB
Critical Path	16.7 nsec
Technology	0.18 μm CMOS
INL	0.39 LSB
DNL	0.43 LSB
Core Area	0.35mm^2

Figure 8 illustrates the dynamic power consumption against the ADC resolution.

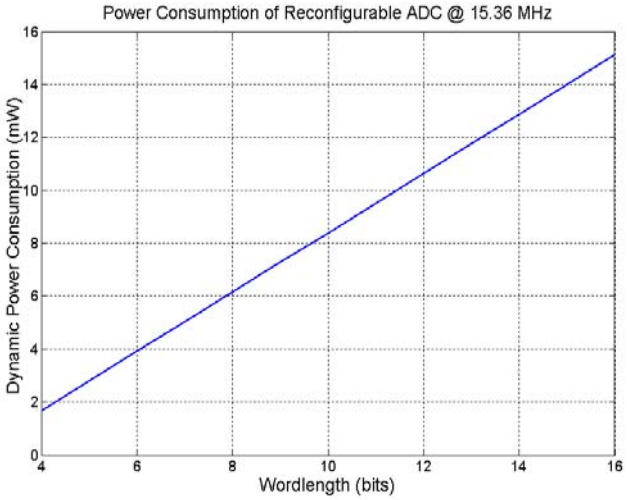

Figure 8. Dynamic Power Consumption of ASIC components in ADC at 15.36 MHz

It is clear that as the word length increases, the power consumption increases proportionally. The power consumption ranges from 1.68Mw to 15.12Mw for word lengths of 4 bits to 16 bits respectively. The power

consumed by the new reconfigurable ADC architecture can be given by:

$$P_{ADC} = \left(\frac{n}{\xi}\right) P_{BLOCK} + P_{S/H} + P_{DEC} \quad (4)$$

where n is the scalable word length, P_{BLOCK} is the dynamic power consumption of a specific ADC block of ξ bits, $P_{S/H}$ is the power consumed by the front end S/H, and P_{DEC} is the power consumed by the digital error correction circuit. Table 3 tabulates the power consumption for the variable word length ADC. A maximum power reduction of 88.89 % has been recorded excluding the DSP control unit, when only 4-bits are required. The average power consumption is 3.92Mw, providing an average power saving of 74.07 %.

Table 3 Power Consumption of Reconfigurable ADC

Resolution (Bits)	Power Consumption (Mw)	Power Saving (%)
4	1.68	88.89
5	2.80	81.48
6 (average)	3.92	74.07
7	5.04	66.67
8	6.16	59.26
9	7.28	51.85
10	8.40	44.45
11	9.52	37.04
12	10.64	29.63
13	11.76	22.22
14	12.88	14.81
15	14.02	7.41
16	15.12	0.00

4. Conclusion

A low power reconfigurable architecture for UTRA-TDD was presented. It consists of a pipeline ADC and control unit. The reconfigurable topology consists of a DSP intelligent control unit and an ASIC. It employs a pipeline ADC, which could be scaled to different resolutions, dependant on in-band and out-of-band power ratios. If out-of-band powers are low, then the word length can be reduced resulting in large power savings. In addition, power dissipation savings were presented along with discussions. It can be said that this architecture will vastly reduce the power consumption compared to a fixed word length ADC when large stop-band attenuations are not always required.

5. References

[1] H. Heikkinen, H. Haas, G.J.R Povey, "Investigation of Adjacent Channel Interference in UTRA-TDD System", IEE Colloquium on UMTS Terminals and Software Radio, 1999.

[2] 3GPP, Technical Specification Group (TSG), Radio Access Network (RAN), Working Group 4 (WG4), 'Evaluation of up– and downlink adjacent channel performance' TSGR4#2(99) 048, February 1999.

[3] Povey, G. J. R., Nakagawa, M. 'A review of Time Division Duplex – CDMA techniques' Proceedings of ISSSTA'98 International Symposium on Spread Spectrum Techniques and Applications. Vol.2., pp. 630-633, 1998.

[4] A. Stojcevski, R. Veljanovski, J. Singh, M. Faulkner, and A. Zayegh, "A Highly Efficient Reconfigurable Architecture for an UTRA-TDD Mobile Station Receiver," Accepted for publication at IEEE ISCAS'2003.

[5] A. Stojcevski, H. P. Le, J. Singh, A. Zayegh, "Flash ADC Architecture", IEE Journal, Electronic Letters, Vol. 39, No. 6, pp. 501-502, 2003.

[6] Stojcevski A, Singh A and Zayegh A, 'Reconfigurable ADC for 3-G UTRA-TDD Mobile Receiver', Proceeding of IEEE, Southwest Symposium on Mixed-Signal Design, SSMSD'03, Navada, Las Vagas, USA, Feb. 2003.