RECONFIGURABLE ADC FOR 3-G UTRA-TDD MOBILE RECEIVER

Aleksandar Stojcevski, Jugdutt Singh and Aladin Zayegh

Centre of Telecommunications & Microelectronics, Victoria University
P.O. BOX 14428, Melbourne City, MC, Victoria 8001, Australia
Email: aleks@sci.vu.edu.au

ABSTRACT

A novel reconfigurable architecture has been proposed for a mobile terminal receiver that can reduce power dissipation dependant on adjacent channel interference. Quantisation error analysis was carried out in order to find the minimum number of bits required. The proposed design can automatically scale the number of bits by monitoring the in-band and out-of-band powers. The new architecture performance was evaluated in a simulation UTRA-TDD environment because of the large near far problem caused by adjacent channel interference from adjacent mobiles and base stations. The UTRA-TDD downlink mode was examined statistically and results show that the reconfigurable architecture can save an average of up to 75% power dissipation when compared to a fixed word length of 16 bits. This will prolong talk and standby time in a mobile terminal. The average number of bits were calculated to be 10, for an outage of 97%.

I. INTRODUCTION

This paper proposes a new low-power reconfigurable architecture for the front end of a mobile terminal receiver, Fig 3. The architecture consists of a variable word length pipelined analog-to-digital converter (ADC). The word length depend on the amount of interference experienced at certain times. When adjacent channel interference (ACI) is low, the required number of word length (bits) are reduced which leads to lower power consumption. Low power consumption is desirable in battery-powered terminals to increase talk and standby times. This reconfigurable system can be applied to various mobile standards by altering the bit values and the controlling code of the ADC. A UMTS terrestrial radio access (UTRA) system was chosen to demonstrate the power saving capabilities of this new reconfigurable design. UMTS includes two duplex modes, frequency division duplex (FDD) and time division duplex (TDD). Fig. 1 presents the two UTRA modes.

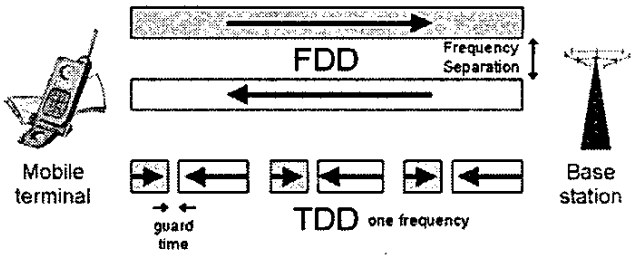

Fig. 1. UTRA-TDD and UTRA-FDD modes

In UTRA-FDD, the uplink and downlink transmissions use two separated radio frequency bands. In UTRA-TDD, uplink and downlink transmissions are carried over same radio frequency by using synchronised time intervals. Time slots in the physical channel are divided into transmission and reception part. Information on uplink and downlink are transmitted reciprocally [1]. This makes TDD mode susceptible to ACI as nearby mobile stations (MS) and base stations (BS) cause interference to each other depending on frame synchronisation and channel asymmetry. This paper presents results for downlink UTRA-TDD operation due to its near far problem. Fig. 2 presents a multi-operator downlink ACI scenario in UTRA-TDD.

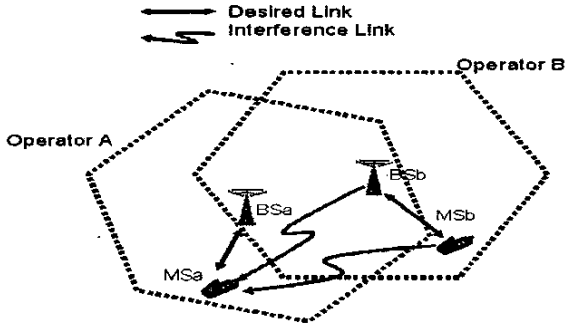

Fig. 2. Downlink ACI scenario in UTRA-TDD

Two interference sources exist in the downlink: adjacent MS and adjacent BS. The interference overlaps are BS→MS and MS→MS.

If adjacent operators have synchronised frames and employ the same asymmetry, it would eliminate MS→MS interference. This cannot be assumed in practice and hence interference is experienced from both sources dependant on frame synchronisation and asymmetry.

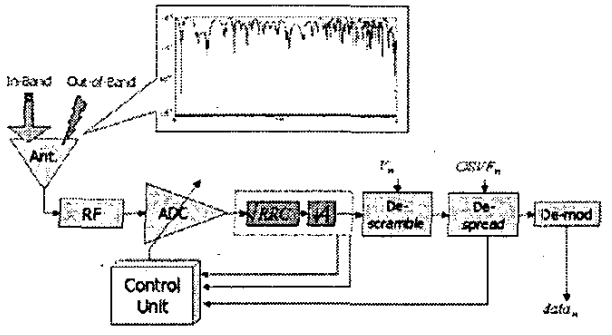

Fig. 3. UTRA-TDD Mobile Station Receiver Block Diagram

II. SIMULATION PLATFORM

The cell topology presented in Fig. 4 is applied. The distance between the COI (shaded cell) BS and the immediate adjacent channel BS along the *a* axis is 50 meters. Parameters used in this work are presented in Table I.

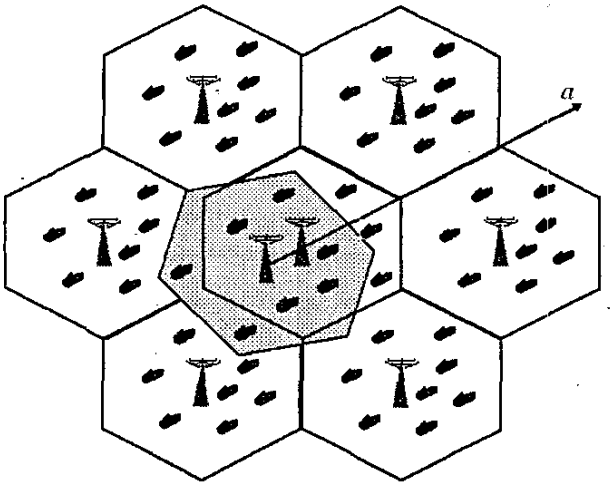

Fig. 4. Cell topology where multiple cells are causing ACI at a target cell on top of the interference cell cluster.

The layer of interfering hexagon cells was approximated with seven cells as it was found that beyond these cells the caused interference was insignificant [2]. The BSs were located in the center of the cells.

The required Eb/No might seem low, but this is due to the assumption of powerful coding mechanism, such as turbo coding. The inherent assumption was that UTRA-TDD is primarily used for data-oriented services.

TABLE I.
SIMULATION PARAMETERS

Parameter	Value
Bit Rate	16 Kbits/s
Max TX Power (dBm)	Downlink: 10, Uplink: 4
Thermal Noise (dBm)	-102.85
Required Eb/No (dB)	3.5
Receiver Sensitivity, without Imargin (dBm)	-112.89
Lognormal Shadowing variable σ (dB)	12
Cell Radius (m)	100
# of Interfering Adjacent Cells	7
# of users in each Interfering Adjacent Cell	8
Synchronisation factor α	Uniform random 0 to 1
Path loss exponent γ	3.0
Full Scale input Voltage V_{fs}	2

III. QUANTISATION ERROR ANALYSIS

This section of the paper derives the amount of quantisation error (QE) permitted at any given location in the COI. The QE value obtained is used to determine the word length of the ADC. The downlink model for the *Eb/No* is similar to that in [3] and is:

$$Eb/No = \frac{Prx^i pg}{Prx^i(M-1) + I_{ad}{}^i + \eta + QE^i} \quad (1)$$

where Prx^i is the received desired signal power at the i^{th} MS in the COI. This is determined by the transmission power of the BS divided by the path loss of the i^{th} MS. BS transmission power is determined by the MS that experiences the greatest path loss.

The same transmission power is then applied to each user within the same time slot. This ensures that the required *Eb/No* can be satisfied for all *M* users. $Prx^i(M-1)$ is intra-cell interference and $I_{ad}{}^i$ is the ACI received after applying a certain Adjacent Channel Protection (ACP) factor:

$$I_{ad}{}^{i} = \frac{I_{total}}{ACP^{i}} \quad (2)$$

where QE is the quantisation error noise. Solving (1) for QE results in:

$$QE^{i} = \left(\frac{\Pr x^{i} pg}{Eb/No}\right) - \left(\Pr x^{i}(M-1) + I_{total}{}^{i} + \eta\right) \quad (3)$$

In order to obtain the word length of the ADC, the calculated QE is substituted in the following equation:

$$n^{i} = \log_2\left(\frac{V_{fs}}{QE^{i}}\right) \quad (4)$$

where n^{i} is the word length of the ADC at a given location in the COI that satisfies the *Eb/No*, V_{fs} is the full scale input voltage of the ADC. Fig. 5 presents the CDF of the QE. Uniform random α values were generated on each Monte Carlo run. Lognormal shadowing of 12dB was used.

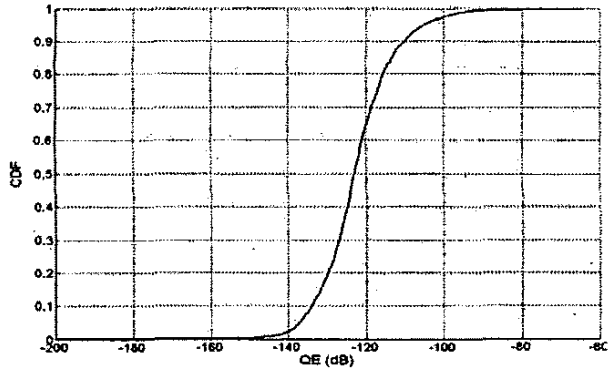

Fig. 5. CDF of QE

The QE was easily converted to the corresponding word length values. Fig. 6 illustrates the CDF of the ADC word length values.

To calculate the average number of bits that will be used, the following calculations are performed:

$$Bits_{average} = \sum_{1}^{n}\left(\frac{(Percentage_B(n) \bullet W_{length}}{100}\right) \quad (5)$$

where $Percentage_B(n)$ is the percentage of the time the ADC has a word length of n (calculating vertically from the CDF) and W_{length} is the word length. Solving (5) yields an average word length of 6 bits. This is a major improvement compared to a fix word length of 16 bits.

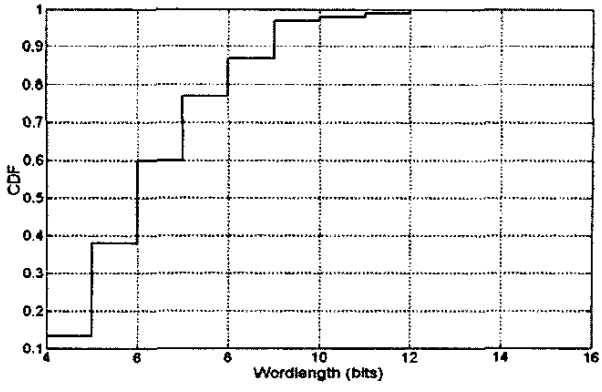

Fig. 6. CDF of ADC word lengths

Further analysis was required to determine the minimum word length the ADC can use to ensure the QoS requirement in met. The QE is mathematically calculated as follows [4]:

$$QE = 10 \bullet \log 10\left(\frac{LSB}{\sqrt{12}}\right) \quad (6)$$

where *LSB* is:

$$LSB = \frac{V_{fs}}{2^{n}} \quad (7)$$

and n is the word length. The above formula was used to calculate the QE for each word length from 1 to 16 bits.

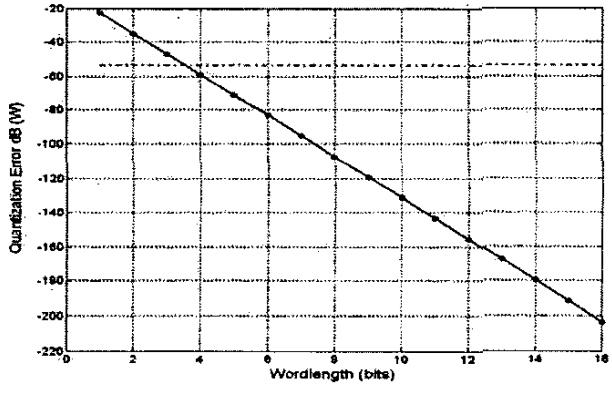

Fig. 7. Quantisation Error vs. Word Length

A V_{fs} of 2 volts was used. Fig. 7 illustrates the results. A safety margin of 1 bit (6dB per bit) would be acceptable and this leads to −12.5dB of QE. Therefore, acceptable word lengths are ≥ 4. The minimum word length is 4.

IV. PROPOSED RICONFIGURABLE ADC TOPOLOGY

The reconfigurable ADC circuit employs the pipeline topology. The architecture is controlled and scaled through the system controller, as shown in Fig 3. Fig 8 shows the topology of the entire reconfigurable system. The system employs thirteen pipeline blocks.

The first block outputs 4 bits and the remaining twelve blocks output 1 bit each. Within each of these stages, a 1.5-bit pipeline topology is used, consisting of a sub-ADC, sub-DAC, a gain amplifier and a sample-and-hold (S/H) circuit. The sub-ADC used is a modified flash topology [5].

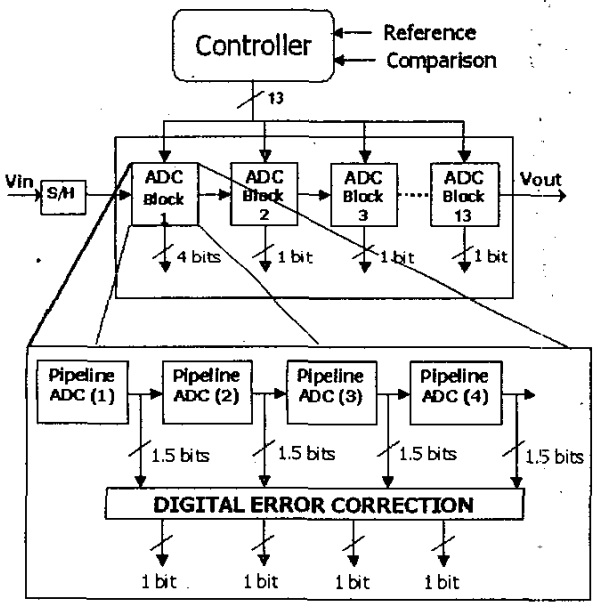

Fig. 8. Reconfigurable Pipeline ADC System

After analysing the different digital error correction (DEC) circuit architectures, the 1.5-bit/stage DEC scheme was found optimal for a low power, high throughput ADC. The overall system design and results of the DEC in this paper are based on a maximum 16-bit ADC.

V. POWER SAVING ANALYSIS

An estimate of the power consumed by the new reconfigurable ADC architecture is given by:

$$P_{ADC} = \left(\frac{n}{\delta}\right) P_{BLOCK} + P_{DSP} + P_{S/H} + P_{DEC} \quad (8)$$

where n is the scalable word length, PBLOCK is the dynamic power consumption of a specific ADC block of δ bits, P_{DSP} is the power dissipated by the DSP proportional to the number of instructions, $P_{S/H}$ is the power consumed by the front end S/H, and P_{DEC} is the power consumed by the digital error correction.

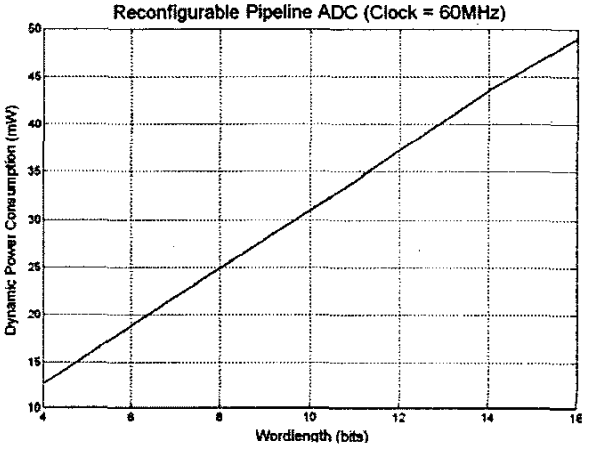

Fig. 9. Power Consumption for various word lengths (excluding DSP)

TABLE II.
POWER CONSUMPTION OF ADC

Scalable Word length	Corresponding Power Consumption Reconfigurable (mW ex DSP)	Standard 16-bit topology (Power Consumption)	Power Savings %
4	12.74	49.62	75
5	15.85	49.62	68
6	18.96	49.62	62
7	21.98	49.62	56
8	25.1	49.62	50
9	28.11	49.62	43
10	31.22	49.62	37
11	34.24	49.62	31
12	37.36	49.62	25
13	40.47	49.62	19
14	43.49	49.62	12
15	46.61	49.62	6
16	49.62	49.62	0

Table II tabulates the power consumption for variable word lengths. A maximum power reduction of 75 % has been recorded excluding the DSP control unit, when only 4-bits are required.

The average power consumption is (18.96mW + P_{DSP}). Power consumption as a function of number of bits is represented by the graph of Fig 9. The graph shows a linear relationship between the number of bits and power consumption.

VI. CONCLUSION

A novel reconfigurable architecture was presented. The architecture consists of a digital filter and an ADC. The filter architecture utilises a DSP core and ASIC. It employs a folded FIR structure and automatically shaves off and adds taps to the ends of the impulse response. This is dependant on the in-band and out-of-band power ratios. This results in lowering or raising the stop band dB level. The ADC topology consists of a DSP intelligent controller and an ASIC. It employs a pipeline ADC, which could be scaled to different resolutions, depending on the ACI. If out-of-band powers are low, then the word length and filter lengths can be reduced resulting in large power savings.

In addition, a power dissipation estimation was presented along with discussions. It can be said that this architecture will vastly reduce the power consumption compared to a fixed length filter structure and fixed word length ADC when large stop-band attenuations are not always required.

This document also examines downlink adjacent interference analysis to support the need for the reconfigurable architecture. It was found that fixed lengths for the filter and ADC are power inefficient. To optimise efficiency for low power drain, not only does the architecture need to employ scalable lengths, it also needs to employ a DSP core controller with advanced power management properties. An average of up to 75% power reduction is available for a 3G UTRA-TDD system. The reduction is likely to be higher for the FDD system because MS→MS ACI does not exist in this duplex mode.

A few assumptions have been made in the interference analysis. Handover was not assumed and mobiles were allocated to base stations based on minimum distance. Handover may reduce the amount of interference experienced and lead to lower filtering and word length requirements. In addition, the same bit rate for each user was assumed. A time slot was near fully loaded by eight users. In practice, a time slot can be fully loaded by one user requiring high data rate. This case might reduce the amount of interference experienced.

VII. REFERENCES

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