

# PERFORMANCE ANALYSIS OF A HIGHLY EFFICIENT FLASH ADC

H. P. Le, A. Stojcevski, A. Zayegh and J. Singh

Faculty of Science, Engineering and Technology, Victoria University  
PO Box 14428, Melbourne City MC 8001, Victoria, Australia

**Abstract** : This paper presents a 2.5V 4-bit highly efficient flash ADC architecture. The design technique of the N-bit modified flash ADC requires only  $2^{(N-2)}+2$  comparators as compared to  $(2^N-1)$  comparators used in a standard N-bit flash converter. A detailed analysis on the modified flash ADC has been presented, which includes speed, complexity and noise. For comparison reasons, the modified flash ADC architecture is operated at 400 MHz, consumes a total power of 7.46mW, and generates total noise power of  $4.86 \cdot 10^{-15} \Delta f (V^2)$  at this frequency. Results indicates that 59% power saving is obtained and 53% of die size could be saved at 400MHz when the modified flash ADC is used instead of a full flash ADC. Such ADC is the best candidate for many applications where power and size are the major factors.

## 1. INTRODUCTION

Many of the communication systems today utilise digital signal processing (DSP) to resolve the transmitted information. Therefore, between the received analog signal and DSP system, an analog-to-digital converter interface is necessary. This interface achieves the digitisation of received waveform subject to a sampling rate requirement of the system. Being a part of communication system, the ADC interface also needs to adhere to the low power constraint [1].

The trend of increasing integration level for integrated circuits has forced the ADC interface to reside on the same silicon with large DSP or digital circuits. By sharing the same supply voltage between ADC and digital circuit, it reduces the overhead cost for extra DC-DC converters to generate multiple supply voltages. Therefore, an ADC operating at the same voltage with the digital circuit is desirable [2].

With the continuous progress of semiconductor technology and scaling of devices, digital circuits have achieved both high speed and low power dissipation. This trend has several impacts on mixed-signal integrated circuits (ICs). First, increasingly additional operations are performed by digital circuits rather than by their analog counterparts. Second, the speed of the ADC and DAC interfaces must scale with the speed of the digital circuits in order to fully utilise the advanced technologies. Third, cost and performance make it desirable to achieve the high levels of integration on a single chip for mixed-signal processing systems [3].

In general, analog-to-digital converters require higher power consumption and circuit complexity than digital-to-analog converters to achieve a given resolution and speed. Therefore, ADCs often appear as the bottleneck in high performance mixed-signal systems [4].

In this paper, design and simulation results of a 4-bit low cost flash ADC are presented. The device is tested and compared with the standard flash ADC

architecture and the results demonstrate the superiority of the modified ADC architecture.

The paper is organised as follows: Section 2 discusses the design of the modified flash ADC Architecture. The noise analysis for the proposed ADC is discussed in Section 3. Simulation results are presented in Section 4. Finally conclusions are drawn in Section 5.

## 2. MODIFIED FLASH ADC DESIGN

Flash ADCs are very fast with typical sampling speed ranging from 20 MS/s to 1G/s, with 4 to 8-bit resolution. The major disadvantages of the full flash ADC architectures are high device power consumption, high device complexity and high device input capacitance. Also, it is practically impossible to implement high resolution flash ADC (beyond 8 bit) due to huge number of comparator required .

When speed is the first priority in the design process of an ADC, flash topology ADC is considered as first choice, but when we add the complexity of the flash ADC, we are forced to compromise between performance and complexity. The following steps are used to design the new 4-bit flash ADC [5]:

- (i) Start with 6 comparators and label them in ascending order, as shown in Fig. 2. The analog input voltage  $V_{in}$  is connected to the non-inverting inputs of all the comparators and the inverting input of the MSB comparator is set to  $8V_{Ref}/16$ ,  $4V_{Ref}/16$  and  $12V_{Ref}/16$ .
- (ii) The outputs of these 3 comparators are used to control the switches (MUX), which are connected to the appropriate fractions of the reference voltage,  $V_{Ref}$ .
- (iii) The outputs of the comparators (Comp<sub>4</sub>, Comp<sub>5</sub>, Comp<sub>6</sub>) are encoded into appropriate values, as shown in Table 1.

The main advantage of the modified flash ADC approach is the great reduction of the number

comparators, which is most critical and the most area-consuming component in the flash ADC design. For  $N$ -bit of resolution, the modified ADC architecture requires only  $2^{(N-2)}+2$  comparators, comparing to  $2^N-1$  comparators required by the full flash ADC topology. Also, the modified flash ADC requires a much less complex encoder than that of traditional full flash ADC. Moreover, the modified flash approach does not require any other components, such as Digital-to-Analog Converter (DAC), subtractors, amplifiers... as required in subranging ADC architectures.

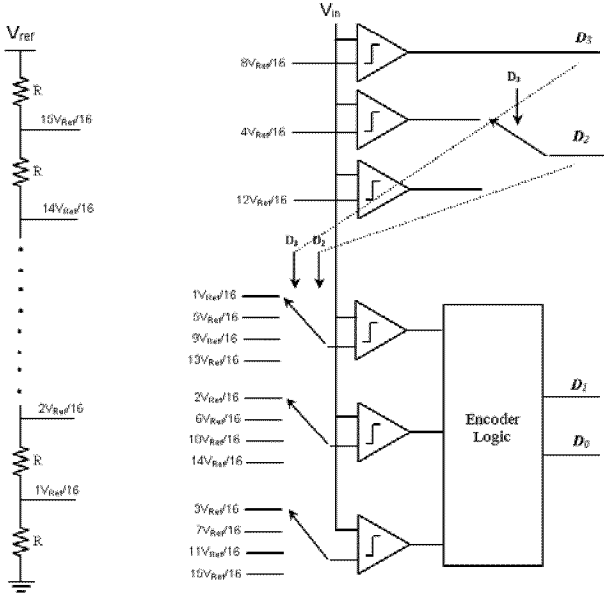


Fig.2: Four-bit Modified Flash ADC.

Table 1: Relationship between comparator outputs and ADC outputs.

O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

$O_2 = 1, O_{12} = 1$      
  $O_2 = 1, O_{12} = 0$      
  $O_2 = 0, O_4 = 1$      
  $O_2 = 0, O_4 = 0$

It should be observed that that we intentionally switch the output of the second comparator ( $comp_2$ ) instead of switching its input in the modified flash ADC. Although a comparator will be saved if we switch the input of  $comp_2$ , the speed of the system will dramatically decrease since the data should be available at the output of  $comp_1$  before the second comparator ( $comp_2$ ) can initiate its comparison. Using the ADC architecture in Fig.2, the first three comparators ( $comp_1$ ,  $comp_2$  and  $comp_3$ ) can perform their comparison simultaneously, and the delay to the selected output is only that of a 2:1 MUX, which is

very small, and hence the system sampling speed will be increased.

Another key characteristic of the proposed ADC architecture in Fig.2 is that it can perform the Analog-to-Digital (A/D) conversion in one clock cycle (like full flash ADC). That is why it is named modified flash ADC. The reasons are described as follows:

- The traditional flash ADC and the proposed modified ADC both employ the dynamic latched-type comparator, described in section 2, which includes an SR latch to keep the comparator output during its recharge-mode. In the traditional full flash ADC topology, to maximise the sampling speed, its 15 comparators perform their comparison simultaneously in the first half clock-cycle, and its logic encoder performs its function in the other half clock-cycle while the comparators maintain their output values (in recharge-mode). Thus, the digital data should be ready after one-clock cycle.

- In the modified flash ADC architecture, as illustrated in Fig. 2, the first three comparators ( $comp_1$ ,  $comp_2$  and  $comp_3$ ) complete the comparison, the 2:1 switches perform the selection and the appropriate reference voltages propagate through the 4:1 switches. In the other half clock-cycle, while all the data are maintained since the first three comparators keep their values in recharge-mode, the bottom comparators ( $comp_4$ ,  $comp_5$  and  $comp_6$ ) perform the comparison and the last two bits ( $D_1$  and  $D_0$ ) will be encoded (since the encoder of the modified flash ADC is very simple). Thus, the digital data is also ready after one clock-cycle.

- Obviously, there will be a slight reduction of the sampling frequency of the modified flash ADC comparing with that of the full flash. Because there will be supplemented delays of the switches and the encoder logic that have to be counted in half clock-cycle. However, the delays of switches are very small (less than 200ps), and thus the sampling frequency reduction is minor.

### 3. 4. NOISE ANALYSIS OF THE MODIFIED FLASH ADC

This section describes the noise analysis of the modified flash ADC.

#### 4.1. Resistor Ladder Noise

In a passive resistor thermal noise is the most dominant source of noise, so here we only consider this type of noise. In a conventional resistor  $R_L$ , the noise source can be represented by a series voltage generator determined by [6]:

$$\overline{V_R^2} = 4kTR_L\Delta f \quad (1)$$

where  $k$  is the Boltzman's constant,  $T$  is the operation temperature,  $R_L$  is the resistor value,  $\Delta f$  is the small bandwidth at frequency  $f$ .

Using equation (1), one resistor in the flash ADC resistor chain ladder generates a noise power of  $1.66 \times 10^{-17} \cdot \Delta f$  ( $V^2$ ). Therefore the entire resistor chain will generate a total noise power of  $2.656 \times 10^{-16} \cdot \Delta f$  ( $V^2$ ).

#### 4.2. 2:1 MUX Noise

The noise generator for a MOS transistor can be expressed as follows [6]:

$$\overline{V_i^2} = \frac{8kT}{3g_m} \Delta f + \frac{K_f}{WLC_{ox}f} \Delta f \quad (2)$$

where  $W$  and  $L$  are the width and length of the MOS transistor, respectively.  $C_{ox}$  is the oxide capacitance.

From the mathematical analysis on the 2:1 MUX, the total output noise current is shown in equation (3).

$$\begin{aligned} \overline{i_{MUX2}^2} &= g_{m5}^2 \overline{V_5^2} + g_{m4}^2 \overline{V_4^2} + g_{m3}^2 \left( \overline{V_3^2} + r_{o1}^2 g_{m1}^2 \overline{V_1^2} + g_{m2}^2 \overline{V_2^2} r_{o2}^2 \right) \\ &+ g_{m6}^2 \left( \overline{V_6^2} + r_{o1}^2 g_{m1}^2 \overline{V_1^2} + g_{m2}^2 \overline{V_2^2} r_{o2}^2 \right) \end{aligned} \quad (3)$$

where  $\overline{V_i^2}$  ( $i = 1 \dots 6$ ) is the noise source generator of transistor  $M_i$  which can be calculated by (2). From equation (3) we can calculate the input noise generator of the 2:1 MUX:

$$\overline{V_{MUX2}^2} = \overline{i_{MUX2}^2} (r_{o3} // r_{o4})^2 = \overline{i_{MUX2}^2} \left( \frac{r_{o3} \cdot r_{o4}}{r_{o3} + r_{o4}} \right)^2 \quad (4)$$

Using equation (4), one 2:1 MUX generates a total noise power of  $4.41 \times 10^{-16} \cdot \Delta f$  ( $V^2$ ) at an operating frequency of 400 MHz. Therefore the total noise power generated by the two 2:1 MUX is  $8.82 \times 10^{-16} \cdot \Delta f$  ( $V^2$ ).

#### 4.3. CMOS Comparator Noise

In the same design structure, the CMOS voltage comparator was analysed for noise. The input noise generator for one comparator can be described as:

$$\begin{aligned} \overline{V_{comp}^2} &= \left( \frac{g_{m1}}{g_{m2}} \right)^2 \overline{V_1^2} + 2\overline{V_2^2} + 2 \left( \frac{g_{m4}}{g_{m2}} \right)^2 \overline{V_4^2} + 2 \left( \frac{g_{m6}}{g_{m2}} \right)^2 \overline{V_6^2} + 2 \left( \frac{g_{m8}}{g_{m2}} \right)^2 \overline{V_8^2} \\ &+ 4 \left( \frac{g_{m10}}{g_{m10} + g_{m14}} \right)^2 \overline{V_{10}^2} + 4 \left( \frac{g_{m14}}{g_{m10} + g_{m14}} \right)^2 \overline{V_{14}^2} \end{aligned} \quad (5)$$

Using equation (5) one comparator generates a total noise power of  $5.3 \times 10^{-16} \cdot \Delta f$  ( $V^2$ ) at an operating frequency of 400 MHz. Therefore the total noise power generated by six comparators working full time will be  $3.18 \times 10^{-15} \cdot \Delta f$  ( $V^2$ ).

The probability of each of these comparators is calculated mathematically in order to find out how much of the load each comparator carries. To calculate the probability of each comparator a sine wave with a 0V to 1V peak-to-peak input has been applied to the

new flash ADC. The probability that comparator 1 outputs a '1' can be described by the following model:

$$P(\text{Comp}_1 = '1') = \text{the fraction of time in 1 period that } V_{in} \geq 0.25 V = t [V_{in} \geq 0.25 V] \quad (6)$$

In similar manor the probability of the rest of the comparators switching were calculated. Table 2 shows the probability switching of all six comparators.  $P(\text{Output} = '1')$  describes the probability that a certain comparator output is on, and  $P(\text{Output} = '0')$  describes that a comparator output is zero.

Table 2: Probability of each comparator

Comparator number	P(Output = '1')	P(Output = '0')
Comp <sub>1</sub>	0.75	0.25
Comp <sub>2</sub>	0.5	0.5
Comp <sub>3</sub>	0.25	0.75
Comp <sub>4</sub>	0.707	0.293
Comp <sub>5</sub>	0.5	0.5
Comp <sub>6</sub>	0.293	0.707

The probability of a certain comparator being on or off will affect the noise that the new flash ADC will generate. From the probability analysis of each comparator, it can be stated that the six comparators are equivalent to three of the comparators working full time. Therefore the total noise power generated is:

$$\begin{aligned} \text{Noise Power} &= \frac{3.18 \times 10^{-15} \cdot \Delta f}{2} (V^2) \\ &= 1.59 \times 10^{-15} \cdot \Delta f (V^2). \end{aligned} \quad (7)$$

In a same manner, all corresponding circuits within the modified-flash ADC were investigated and analysed for their noise contributions to the device. Table 3 shows a summary of the noise analysis for each component within the new flash ADC architecture. The total noise power is also calculated and presented in this table.

Table 3: Summary of noise power in the proposed ADC.

	Noise in one component	Number of components	Total Noise in specific components
<b>Resistor</b>	$1.66 \times 10^{-17} \cdot \Delta f$	16	$2.65 \times 10^{-16} \cdot \Delta f$
<b>2:1 MUX</b>	$4.41 \times 10^{-16} \cdot \Delta f$	2	$8.82 \times 10^{-16} \cdot \Delta f$
<b>4:1 MUX</b>	$7.07 \times 10^{-16} \cdot \Delta f$	3	$2.12 \times 10^{-15} \cdot \Delta f$
<b>Comp.</b>	$5.30 \times 10^{-16} \cdot \Delta f$	3 (operating full time)	$1.59 \times 10^{-15} \cdot \Delta f$
<b>Total Noise</b>			$4.86 \times 10^{-15} \cdot \Delta f$

## 4. SIMULATION RESULTS

The full flash ADC and the modified flash ADC have been implemented and simulated in Cadence Analog

Environment, and comparison of their performance has been made. Fig. 3 presents the plots of differential nonlinearity (DNL) and integral nonlinearity (INL) errors of the modified flash ADC at 400MHz sampling frequency. It can be seen that the DNL and INL achieved are 0.36 and 0.41 LSB respectively.

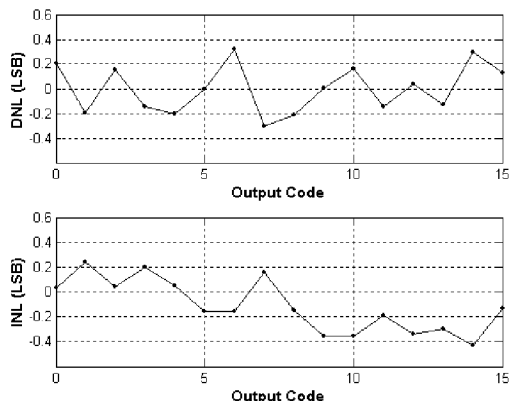


Fig. 3: DNL and INL at 400MHz.

Table 4 summarizes the performance of the two ADC approaches, including the power consumption of the resistor ladders. If this new design was employed within a wireless application (i.e. Wide Band CDMA) then a typical  $\Delta f$  value will be 5MHz. Therefore the total noise power of the system will be  $2.43 \times 10^{-8} (V^2)$ .

Table 4: Comparison results of the ADC circuits performance

Description	4-bit Full Flash	4-bit Modified Flash
<b>Number of Devices</b>		
NMOS	179	84
PMOS	194	90
Resistors	16	16
<b>Power Consumption</b>	18.26 mW	7.46 mW
<b>Speed</b>	400 MHz	400 MHz
<b>Noise Power (<math>\Delta f = 5 \text{ MHz}</math>)</b>		$2.43 \times 10^{-8} V^2$
<b>Resolution</b>	4 bits	4 bits
<b>Voltage Supply</b>	2.5 volts	2.5 volts

As mentioned earlier, the comparator is the most critical and the most area-consuming component of the flash ADC design. Fig. 4 shows a comparison of the number of comparators required for the two different flash ADC circuits.

From this analysis, we can conclude the advantages of the modified flash ADC architecture, which include, less components therefore smaller size, and lower power consumption. These characteristics make this new device better candidate for many applications where power and size are the major factors.

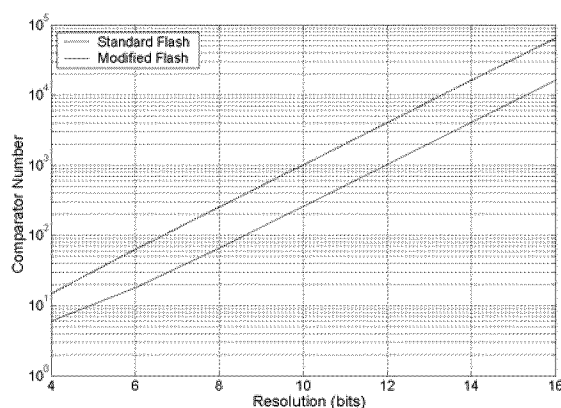


Fig. 4: Number of Comparators required for each Flash design.

## 5. CONCLUSION

A 4-bit, CMOS modified flash ADC has been presented, which requires only  $2^{(N-2)} + 2$  comparators to implement an N-bit ADC. This approach greatly reduces the complexity of the full flash ADC. The final modified flash ADC dissipates only 7.46mW of power as compared to a full flash ADC of 18.26mW.

Results indicate that a 59% power saving is obtained and 53% of die size could be saved when the modified flash ADC is used instead of a full flash ADC. For comparison reasons the two analog-to-digital converters were operated at a speed of 400 MHz.

## 7. REFERENCES

- [1] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE Journal of Solid State Circuits*, vol. 34, pp. 699-706, 1999.
- [2] T. B. Cho, D. W. Cline, S. G. Conroy, and P. Gray, "Design Considerations for Low- Power, High-Speed CMOS Analog/Digital Converters," *In Proceedings of the IEEE Symposium on Low Power Electronics*, pp. 70-73, 1994.
- [3] F. Maloberti, "High Speed Data Converters and New Telecommunication Needs," *In Proceedings of Southwest Symposium on Mixed-Signal Design*, pp. 147-150, 1999.
- [4] A. Stojcevski, J. Singh, and A. Zayegh, "Design Implication of the Building Block Components of Pipeline Analog-to-Digital Converters," *Advances in Modeling & Simulation, AMSE Journal Press.*, 2002.
- [5] A. Stojcevski, H. P. Le, A. Zayegh, and J. Singh, "High Performance Flash ADC with Reduced Power and Complexity in a Simulation Environment," presented at the Mediterranean Conference on Modelling and Simulation (MCMS'03), Reggio Di Calabria, Italy, 2003.
- [6] P. G. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*: Forth Edition, John Wiley & Son Inc., 2001.