Noise Analysis of a Reduced Complexity Pipeline Analog-to-Digital Converter

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Abstract

This paper presents a mathematical analysis of the noise generated within a 12-bit reduced complexity pipeline Analog-to-Digital converter (ADC) to demonstrate the effect of noise on the device performance. A modified flash ADC was employed instead of the traditional full flash ADC to implement the sub-ADC in the proposed pipeline ADC to reduce the device complexity and attain lower system power consumption. The 12-bit pipeline ADC is operated at 400MHz and generates total noise power of $3.38\times10^{-12}\cdot\Delta f$ (V^2) at this frequency. The developed model provides a good estimation of the noise generated by the circuit and gives an accurate prediction on the circuit noise performance. Also, such model provides good guide for further improvement of the circuit performance.

1. Introduction

Analog-to-Digital converters (ADCs) are the most essential part in any signal processing systems and other data acquisition systems because they are the boundary between the analog and digital signal processing. The function of an ADC is to transform an analog signal into equivalent digital data for further storage and processing. Since the mid-1970s, ADCs have been widely designed using integrating, successive approximation, flash, delta-sigma techniques. More recently, there has appeared a new class of ADC with an architecture known as pipeline, which offered an attractive combination of high speed, high resolution, low power dissipation and small die size. The pipeline ADC, therefore, became the optimum solution for present low power applications, such as a wireless communication system [1].

However, when working at high frequencies, the noise generated within the pipeline ADC itself will play an increasingly important role in its overall performance. The existence of noise in CMOS integrated circuits is basically due to the fact that electrical charge is not continuos but is carried in discrete amounts to the electron charge, and thus noise is associated with fundamental processes in the integrated-circuit devices [2]. A detailed analysis on the noise performance of the device, therefore, is essential.

Fig 1 shows a typical pipeline scheme. A pipeline ADC basically consists of numerous consecutive stages, each stage contains a sub-ADC, an inter-stage sample-and-hold circuit (SHC), a sub-digital-to-analog converter (sub-DAC), and a substractor that includes an amplifier to provide gain, as illustrated in Figure 1. Each stage generates a coarse m_i-bit. The final stage, however, only includes an inter-stage SHC and a fine ADC since no analog conversion will be required [3]. To obtain 12-bit resolution, the pipeline ADC is designed to have three stages, each stage contributes 4-bit resolution.

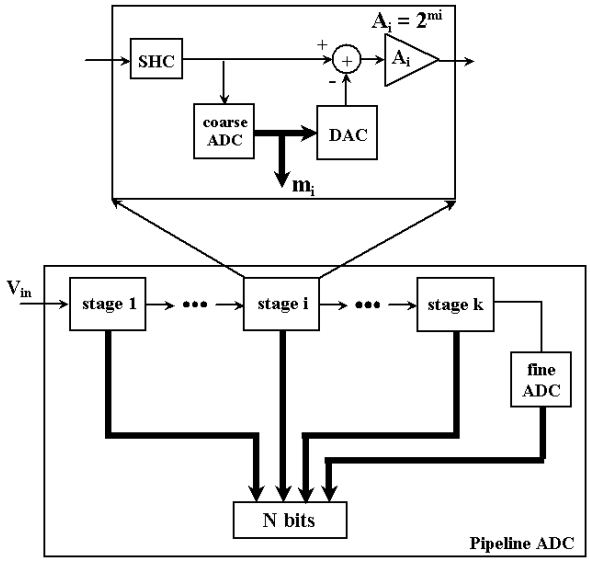

Figure 1. Pipeline ADC Architecture

This paper presents a mathematical model of noise in a 12-bit pipeline ADC to demonstrate the effect of noise on the device performance. The model provides the

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estimation of the total noise that will be generated by the device, and thus it will give a prediction on the circuit noise performance.

2. Implementation of the Building Block Components for a Pipeline ADC

Figure 2 shows the detailed implementation of a 4-bit single stage utilised the designed 12-bit pipeline ADC. It incudes a sub-ADC, an inter-stage SHC, a sub-DAC, and a substractor that includes an amplifier to provide gain The details of the design of building block components of the 4-bit single stage are discussed as follows:

- **Sub-ADC:** Flash ADCs are typically employed as coarse and fine ADCs in a pipeline ADC architecture. In this pipeline ADC scheme, a modified flash ADC [4] was used instead of the traditional full flash ADC to reduce design complexity and power dissipation. The modified flash ADC, which utilised an optimised latched-type comparator [5], can perform the Analog-to-Digital (A/D) conversion in one clock cycle (like a full flash ADC). The main advantage of the modified flash ADC is the great reduction in the number of comparators, and therefore the device obtains a great power saving and size reduction. Thus, the designed 12-bit pipeline ADC will achieve a great reduction in the device complexity and area [4].

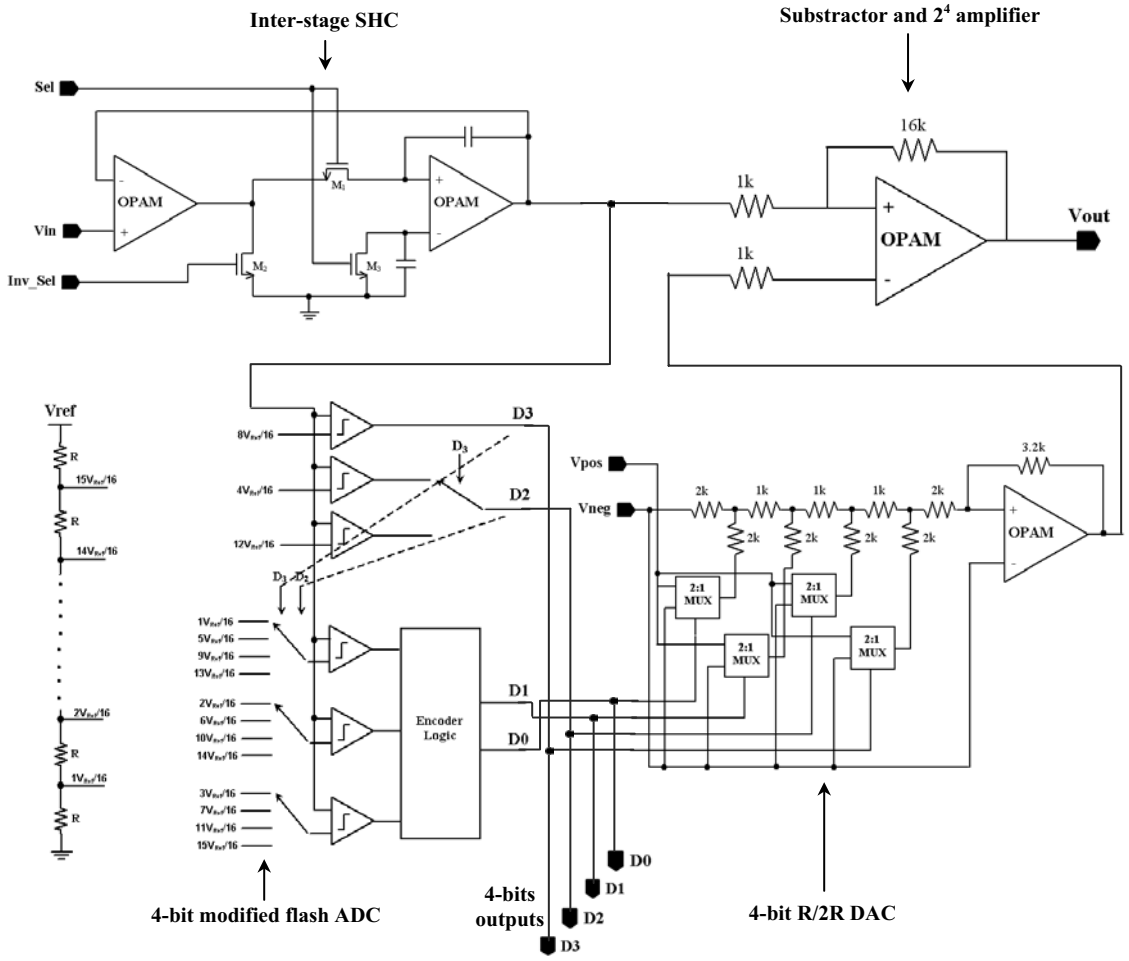


Figure 2. A 4-bit single stage block employed in the pipeline ADC

- **SHC** is an important building block in the pipeline ADC architecture since the system throughput and accuracy are limited by the speed and precision at which the input and residue analog voltages are sampled and held. The inter-stage SHC architecture, utilised in the designed pipeline ADC, is illustrated in Figure 2. It employs the series sampling technique, and the output is fedback to the first OPAM. The main advantages of this architecture is that the charge injection error and the clock

feedthrough error are effectively removed [6], resulting in a very high accuracy.

- The technique used to implement the **sub-DAC** in the single stage pipeline block is R/2R ladder due to its advantages that are simple configuration and only two resistor values required, whose exact values are not critical. Therefore it is well suited to integrated circuit realisation [7]. **The stage substractor and amplifier** was implemented using typical linear amplifier due to its advantages in low design complexity, low power consumption and good accuracy [8].

To obtain 12-bit resolution, the designed pipeline ADC comprises of two 4-bit single stage block, as illustrated in Figure 2, and a fine 4-bit stage which includes only includes an inter-stage SHC and a fine modified flash ADC since no analog conversion will be required.

3. Noise Analysis of the Pipeline ADC

This section describes the noise analysis of the reduced complexity 12-bit pipeline ADC.

3.1. Resistor Noise Analysis

In a passive resistor thermal noise is the most dominant source of noise, so here we only consider this type of noise. In a conventional resistor R_L, as shown in Figure 3, the noise source can be represented by a series voltage generator as [2]:

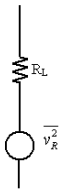


Figure 3. Noise source in resistor

$$\overline{V_R{}^2} = 4kTR_L\Delta f \tag{1}$$

where k is the Boltzman's constant, T is the operation temperature, R_L is the resistor value, Δf is the small bandwidth at frequency f.

3.2. MOS Transistor Noise Analysis

The major noise sources in CMOS transistors are:

- ***Thermal noise***: due to the random thermal motion of electrons (Johnson effect) since the typical electron drift velocities in a conductor are much less than electron thermal noise. This is independent of frequency [6].

$$\overline{V_{THERMAL}^2} = 4kT\frac{2}{3g_m}\Delta f \tag{2}$$

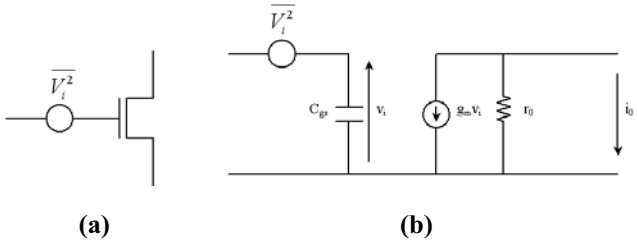
where g_m is the MOS transconductance and Δf is the bandwidth (in Hertz)

- ***Flicker noise (also called 1/f noise)***: caused by traps associated with contamination and crystal defects. This noise is inversely proportional to frequency [6].

$$\overline{V_{FLICKER}^2} = K\frac{I_D^a}{f}\Delta f \tag{3}$$

where I_D is the drain current, K is a constant for a particular device, Δf is the bandwidth (in Hertz) and a is a constant in the range of 0.5 to 2.

Various studies on noise models of MOS transistors have been reported. The most popular noise model of a MOS transistor is shown in Figure 4, where all the noise sources are lumped into an equivalent input noise generator $\overline{V_i^2}$ [2]:



(a) **(b)**

Figure 4. MOSFET equivalent noise generator (a) device symbol (b) equivalent circuit

where:

$$\overline{V_i^2} = \frac{8kT}{3g_m}\Delta f + K\frac{I_D^a}{f}\Delta f \tag{4}$$

The flicker noise component is approximately independent of bias current and voltage. Practical results showed that for a typical MOS transistor, the flicker noise is inversely proportional to the active gate area of the transistor, and it is also inversely proportional to the gate-oxide capacitance per unit area [2]. The noise generator of a MOS transistor, thus, can be expressed as follows:

$$\overline{V_i^2} = \frac{8kT}{3g_m}\Delta f + \frac{K_f}{WLC_{ox}}\Delta f \tag{5}$$

Measurements show that the typical value of K_f is 3×10^{-24} (V^2F) or 3×10^{-12} (V^2pF) [2].

3.3. Sub-ADC Noise Analysis

The modified flash ADC was fully analysed for noise as reported in [9]. At 400MHz sampling frequency, the modified flash ADC generates a total noise power of $4.86\times10^{-15}\cdot\Delta f$ (V^2). Using the same technique as reported in [9, 10], we will analyse the noise in the other building block components in the 12-bit pipeline ADC.

3.4. Sub-DAC Noise Analysis

The 4-bit sub-DAC employed of one OPAM, four 2:1 multiplexers (MUX), five 1kΩ-resistors and five 2kΩ-resistors. Therefore, we have to analyse the noise in each component in the sub-DAC first.

First, the noise analysis of the 2:1 MUX will be considered. A 2:1 MUX basically comprises of six MOS transistors, as illustrated in Figure 5a. As seen in equation (5), each transistor in the 2:1 MUX will contribute a specific value to the entire device noise power. All of these MOS noise sources, however, can be lumped into an equivalent input noise source that will generates an equivalent noise power [10]. Figure 5a shows the 2:1 MUX circuit with noise contribution, and Figure 5b shows the circuit with an equivalent input noise voltage, $\overline{V_{MUX2}^{\ 2}}$.

From the mathematical analysis on the 2:1MUX illustrated in Figure 5a, the total device output noise current is shown in equation (6).

$$\overline{i_{MUX2}^{\ 2}} = g_{m5}^{\ 2}\overline{V_5^{\ 2}} + g_{m4}^{\ 2}\overline{V_4^{\ 2}} + g_{m3}^{\ 2}\left(\overline{V_3^{\ 2}} + r_{o1}^{\ 2}g_{m1}^{\ 2}\overline{V_1^{\ 2}} + g_{m2}^{\ 2}\overline{V_2^{\ 2}}r_{o2}^{\ 2}\right) + g_{m6}^{\ 2}\left(\overline{V_6^{\ 2}} + r_{o1}^{\ 2}g_{m1}^{\ 2}\overline{V_1^{\ 2}} + g_{m2}^{\ 2}\overline{V_2^{\ 2}}r_{o2}^{\ 2}\right) \quad (6)$$

where $\overline{V_i^{\ 2}}$ (i = 1..6) is the noise generator of transistor M_i which can be calculated by (5). r_{oi} (i=1,2) is the output resistance of transistor M_i

By equating the total output noise currents in Figure 5a and Figure 5b, the equivalent input noise generator of the 2:1 MUX can be calculated as follow:

$$\overline{V_{MUX2}^{\ 2}} = \overline{i_{MUX2}^{\ 2}}\left(r_{o3}\,//\,r_{o4}\right)^2 = \overline{i_{MUX2}^{\ 2}}\left(\frac{r_{o3}\cdot r_{o4}}{r_{o3}+r_{o4}}\right)^2 \quad (7)$$

In the similar manner as the 2:1 MUX, an OPAM [11] utilised in the sub-DAC is analysed for noise. By equating the output noise current that is contributed by all the MOS noise sources with the output noise current that is generated by an equivalent input noise source, we can determine the equivalent input noise source of the OPAM as shown in equation (8):

$$\overline{V_{OPAM}^2} = \frac{1}{g_{m1}}\left[29\times\overline{V_1^{\ 2}}\times g_{m1} + 20\times\overline{V_3^{\ 2}}\times g_{m3} + 3\frac{\overline{V_{R1}^{\ 2}}}{R_1}\right] \quad (8)$$

where $\overline{V_i^{\ 2}}$ (i = 1,3) is the noise generator of transistor M_i which can be calculated by (5), $\overline{V_{R1}^{\ 2}}$ represents a passive resistor noise generator calculated by (1).

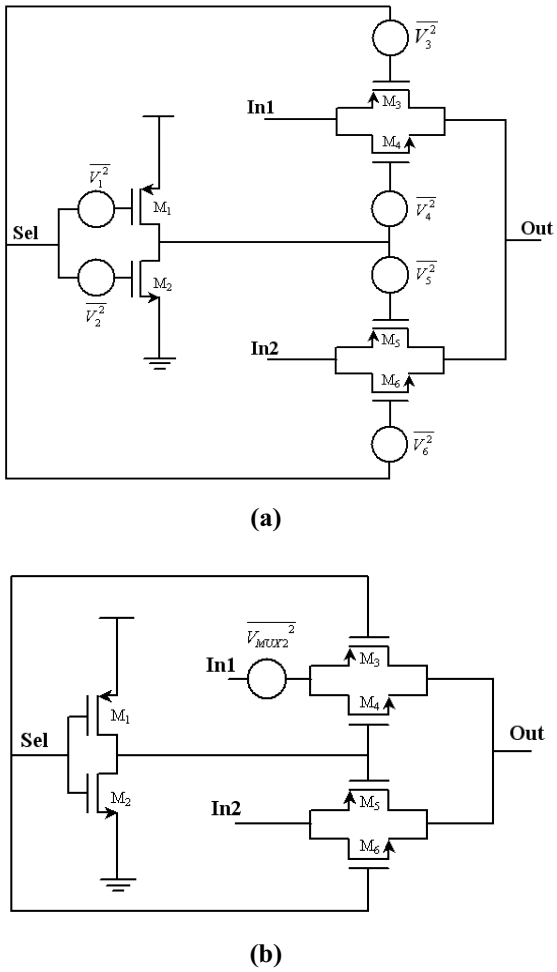


Figure 5. 2:1 MUX (a) with noise generators (b) with equivalent input noise voltage

Using equation (1), at 400 MHz operating frequency, one 1kΩ resistor and one 2kΩ resistor in the sub-DAC will generate a noise power of $1.66\times10^{-17}\cdot\Delta f$ (V^2) and $3.32\times10^{-17}\cdot\Delta f$ (V^2) respectively. Using equation (8), one OPAM in the DAC will generate a noise power of $1.54\times10^{-15}\cdot\Delta f$ (V^2) at an operating frequency of 400 MHz. Using equation (7), one 2:1 MUX in the DAC will

generate a noise power of $4.43\times10^{-16}\cdot\Delta f$ (V^2) at 400 MHz operating frequency.

Therefore the 4-bit sub-DAC will generate a total noise power of $3.56\times10^{-15}\cdot\Delta f$ (V^2) at this frequency.

3.5. Inter-stage SHC Noise Analysis

In the same design structure, the inter-stage SHC will be considered for noise in this section. It comprises of two OPAM and three transistors, as illustrated in Figure 2. Using equation (5), one transistor in the inter-stage SHC stage generates a noise power of $5.90\times10^{-19}\cdot\Delta f$ (V^2) at an operating frequency of 400 MHz. Using equation (8), one OPAM in the designed SHC generates a noise power of $1.54\times10^{-15}\cdot\Delta f$ (V^2) at 400 MHz operating frequency. Therefore the entire SHC will generate a total noise power of $3.07\times10^{-15}\cdot\Delta f$ (V^2) at this frequency.

3.6. Inter-state Amplifier Noise Analysis

In the similar manner, the total noise power generated by the designed inter-stage amplifier is analysed. The amplifier comprises of one OPAM and three resistors (two 1kΩ and one 16kΩ) whose noise power can be determined by equation (8) and (1) respectively. Therefore, the amplifier generates total noise power of $1.84\times10^{-15}\cdot\Delta f$ (V^2) at 400MHz sampling frequency.

4. Results

Table 1 shows a summary of the noise analysis for each stage within the 12-bit pipeline ADC. Since the noise analysis presented in this paper is concentrated on the total noise generated within the ADC itself, it is feasible to assume that the input signal to the 12-bit pipeline ADC is noiseless. In another word, the input noise power to the ADC stage 1 is zero. From the second stage, however, the noise generated within its previous stage will be considered as its input noise power.

In addition, as illustrated in Figure 1, each ADC stage generates two output signals, its output digital signal and an analog signal to the next stage. Therefore, the total noise power seen from a stage output port only includes the noise generated within the SHC and the sub-ADC. While the total noise power delivered to the next stage includes the total noise power of the inter-stage amplifier and the noise power of the sub-ADC, the SHC and the sub-DAC with the amplification factor of 2^4, which is the gain of the inter-stage amplifier.

The total noise power of the ADC is also calculated and presented in this table.

Table 1. Summary of noise power in the designed 12-bit pipeline ADC

Component	Noise in one component	Amplification factor	Noise power to output	Amplification factor	Noise power to next stage
4-bit ADC Stage 1					
Stage Input Noise Power (V^2)	$0\cdot\Delta f$	1	$0\cdot\Delta f$	16	$0\cdot\Delta f$
Coarse ADC (V^2)	$4.86\times10^{-15}\cdot\Delta f$	1	$4.86\times10^{-15}\cdot\Delta f$	16	$7.78\times10^{-14}\cdot\Delta f$
Inter-stage SHC (V^2)	$3.07\times10^{-15}\cdot\Delta f$	1	$3.07\times10^{-15}\cdot\Delta f$	16	$4.91\times10^{-14}\cdot\Delta f$
Sub-DAC (V2)	$3.56\times10^{-15}\cdot\Delta f$	N/A	N/A	16	$5.70\times10^{-14}\cdot\Delta f$
Inter-stage Amplifier (V^2)	$1.84\times10^{-15}\cdot\Delta f$	N/A	N/A	1	$1.84\times10^{-15}\cdot\Delta f$
Noise power to output (V^2)			**$7.93\times10^{-15}\cdot\Delta f$**		
Noise power to next stage (V^2)					**$1.86\times10^{-13}\cdot\Delta f$**
4-bit ADC Stage 2					
Stage Input Noise Power (V^2)	$1.86\times10^{-13}\cdot\Delta f$	1	$1.86\times10^{-13}\cdot\Delta f$	16	$2.98\times10^{-12}\cdot\Delta f$
Coarse ADC (V^2)	$4.86\times10^{-15}\cdot\Delta f$	1	$4.86\times10^{-15}\cdot\Delta f$	16	$7.78\times10^{-14}\cdot\Delta f$
Inter-stage SHC (V^2)	$3.07\times10^{-15}\cdot\Delta f$	1	$3.07\times10^{-15}\cdot\Delta f$	16	$4.91\times10^{-14}\cdot\Delta f$
Sub-DAC (V2)	$3.56\times10^{-15}\cdot\Delta f$	N/A	N/A	16	$5.70\times10^{-14}\cdot\Delta f$
Inter-stage Amplifier (V^2)	$1.84\times10^{-15}\cdot\Delta f$	N/A	N/A	1	$1.84\times10^{-15}\cdot\Delta f$
Noise power to output (V^2)			**$1.94\times10^{-13}\cdot\Delta f$**		
Noise power to next stage (V^2)					**$3.17\times10^{-12}\cdot\Delta f$**
4-bit Fine Stage (final stage)					
Stage Input Noise Power (V^2)	$3.17\times10^{-12}\cdot\Delta f$	1	$3.17\times10^{-12}\cdot\Delta f$	N/A	N/A
Coarse ADC (V^2)	$4.86\times10^{-15}\cdot\Delta f$	1	$4.86\times10^{-15}\cdot\Delta f$	N/A	N/A
Inter-stage SHC (V^2)	$3.07\times10^{-15}\cdot\Delta f$	1	$3.07\times10^{-15}\cdot\Delta f$	N/A	N/A
Noise power to output			**$3.18\times10^{-12}\cdot\Delta f$**		
Total 12-bit pipeline noise (V^2)			**$3.38\times10^{-12}\cdot\Delta f$**		

5. Conclusion

A mathematical model representing noise performance of 12-bit, 3-stage CMOS pipeline ADC has been presented. A modified flash ADC approach has been employed to implement sub-ADCs in the designed pipeline structure to reduce the device complexity and to acquire lower device power dissipation. At operating frequency of 400MHz, the 12-bit pipeline ADC generates a total noise power of $3.38\times10^{-12}\cdot\Delta f$ (V^2). The developed model provides a good estimation of the noise generated by the circuit and gives an accurate prediction on the circuit noise performance. Also, such model provides good guide for further improvement of the circuit performance.

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