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CONTROL UNIT IMPLEMENTATION FOR A REDUCED COMPLEXITY RECONFIGURABLE DATA ACQUISITION ARCHITECTURE

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ABSTRACT

A control unit for a reconfigurable data acquisition (DAQ) architecture has been presented. The reconfigurable DAQ system is employed in a digital relay for power system distance protection. It can detect and adjust its sampling speed depending on the occurrence of a fault in the network. Results indicate that a 98% reduction of average data throughput is achieved 87% reduction of power consumption is obtained and the total sampled data is reduced by 98% when the reconfigurable algorithm is applied. This significantly reduces the system need for data storage, and hence correspondingly reduces the system complexity, and also enables an increase of system detection speed and accuracy.

1. INTRODUCTION

Power systems occasionally experience faults and abnormal conditions, in such cases relays are used to avoid damage to the system and customer equipments. In early development of power systems, protection functions were performed by electro-mechanical relays, which are sill currently used. Recently, digital relays are being increasingly used in power industry due to their advantages that are: digital relays generally use fewer parts, they are not required to be tuned individually to obtain consistent result, they provide remote targets and fault location information to assist operators in restoration of electrical service and system changes can be made simply by changing software only [1, 2]. Traditionally, DAQ systems in digital relays have been built on Printed Circuit Boards (PCBs) with high quality shielding, grounding and insulation, inducing high cost, high power consumption and large size. There is an emerging approach of integrating the complete DAQ system on a single chip, which obtains advantages of higher speed, better accuracy, less computation, cheaper, faster, smaller and less power dissipation. There is, however, a continued search for architectures and circuit techniques enabling DAQ systems to attain higher speed, more enhanced performance with smaller chip area and less complexity [3].

Previous works [4, 5] concentrated on the design, implementation and analysis of constituent elements for a DAQ system. A reduced complexity DAQ system has also been implemented in [6]. This paper focuses on the reconfigurable DAQ architecture and provides an in-depth description of the control unit design along with the system efficiency analysis. The reconfigurable DAQ system can detect and adjust its sampling speed depending on the occurrence of a fault in the network, enabling a large reduction of data throughput and a host CPU processing time saving. This also allows a reduction of the system need for data storage and hence correspondingly reduces the system complexity.

The paper is organised as follows: Section 2 discusses the reconfigurable architecture of the proposed DAQ chip. Section 4 presents the in-depth design and implementation of an intelligent control unit for the proposed reconfigurable architecture. Simulation results will be shown in Section 4. Finally, the conclusion and discussion will be drawn in Section 5.

2. RECONFIGURABLE DAQ SYSTEM ARCHITECTURE

The reconfigurable architecture of a DAQ system is shown in Figure 1. It consists of an intelligent control unit and a full custom DAQ unit with a variable cut-off frequency anti-aliasing filter. The DAQ unit sampling frequency is also variable by changing the system master clock generator [6].

Pipeline ADC architecture is selected because of its optimum balance of size, speed, power dissipation and resolution. In a typical pipeline ADC, flash ADCs are employed to provide coarse and fine resolutions. However, the major disadvantages of the full flash ADC architectures are high power consumption, high complexity and high input capacitance. A modified flash ADC [4, 5], as illustrated in Fig. 6, was used instead of the traditional full flash ADC to reduce design

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complexity and power dissipation. The modified flash ADC, which utilised an optimised latched-type comparator, can perform the Analog-to-Digital (A/D) conversion in one clock cycle (like a full flash ADC). The main advantage of the modified flash ADC approach is the great reduction in the number of comparators. Therefore the device obtains a great power saving and size reduction. To obtain 12-bit resolution, the pipeline ADC is designed to have 3 stages, each stage contributes 4-bit resolution [5].

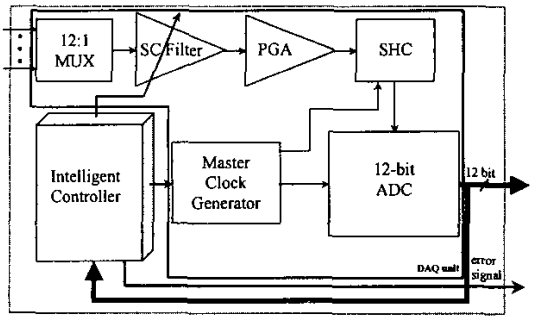

Figure 1. Reconfigurable Architecture

It is uncommon for an anti-aliasing filter to be integrated within a DAQ system. In this designed unit, an on-chip anti-aliasing filter with variable cut-off filter is included allowing the implementation of the reconfigurable property on DAQ unit, which will be discussed thoroughly in the next section. CMOS switched capacitor (SC) filter architecture is selected since it achieves several advantages over its counterparts. It exhibits improved dynamic range, is more capable of handling large signals, and is capable of being programmable by changing its sampling frequency [7]. A SC low pass filter comprising of an inverting integrator and a non-inverting integrator was employed and the transfer function of the filter is described in equation (1) [6].

$$H(s)=\frac{V_0}{V_i}=-\frac{C_4C_6+4\pi^2f^2f_c^2C_1C_3}{C_4C_5+4\pi^2f^2f_c^2C_2C_3} \qquad (1)$$

For power protection applications, very high sampling rate is not always required since the normal line current and voltage frequencies are of 50Hz. Therefore, at the normal operating condition, the reconfigurable DAQ system operates at a low sampling speed and the anti-aliasing filter cut-off frequency is reduced, which leads to a low data throughput and a host CPU processing time saving, allowing reduction of the system need for data storage and hence correspondingly reduce the system complexity.

However, when a fault occurs, the line voltage is reduced to a very low value whist the currents of abnormally high magnitude and high frequency will flow through the network. The DAQ system should be capable of increase its sampling rate in order to not only accurately detect the fault and estimate the fault distance but also capture all the data to be able to analyse the fault.

The intelligent controller is capable of detecting an abnormal condition on the power system network and generates signals to increase sampling speed of the DAQ unit and to increase cut-off frequency of on-chip anti-aliasing filter to capture all high-frequency voltages and currents. It will also generate an "error signal" to notify the central CPU of an abnormal condition detected in the power system.

3. INTELLIGENT CONTROLLER DESIGN

The controller is the intelligence behind the reconfigurable architecture. It continuously monitors the voltages and currents to detect the appearance of an abnormal condition on the power transmission network. Then it will send signals to adjust DAQ system sampling speed and filter cut-off frequency for properly detecting the fault location and properly analysing the fault.

An abnormal condition on the power system can be detected from only three samples. Let v(t-Δt), v(t) and v(t+ Δt) be the three sampled taken at short intervals. The line voltage, then, will be expressed by:

$$v(t)=V_P\sin(\omega t+\phi_V) \qquad (2)$$

where: ω is the line voltage signal frequency, ϕ_V is the voltage signal phase angle.

The voltage differential, thus, can be determined by:

$$v'(t)=\omega V_P\cos(\omega t+\phi_V) \qquad (3)$$

Using trapezoidal rule, v'(t) can be estimated by:

$$v'(t)=\frac{v(t+\Delta t)-v(t-\Delta t)}{2\times\Delta t} \qquad (4)$$

In the similar manner, i'(t) will be evaluated. Hence, the line impedance magnitude can be calculated based on the squares of voltage and current magnitudes as follows [2]:

$$Z_{line}=\sqrt{\frac{v(t)^2+\left(\frac{v'(t)}{\omega}\right)^2}{i(t)^2+\left(\frac{i'(t)}{\omega}\right)^2}} \qquad (5)$$

The impedance phase angle can be found from the formula [2]:

$$\phi_{line}=\arctan\left(\omega\times\frac{i(t)}{i'(t)}\right)-\arctan\left(\omega\times\frac{v(t)}{v'(t)}\right) \qquad (6)$$

Figure 2 shows the flow chat of the reconfigurable algorithm of the DAQ system. At the normal conditions, the designed DAQ system operates at a low sampling speed. Based on the above algorithm the magnitude and phase angle of line impedances will be estimated and compared with typical impedance magnitude and phase angle respectively, allowing a margin for possible measured errors. When an abnormal condition of transmission line is detected, an error will be generated to the cental CPU and the DAQ system will

automatically increase its sampling speed and the filter cut-off frequency so that more data will be available allowing cental CPU to accurately determine the fault location in order to generate trip signals and for later trip signal analysis.

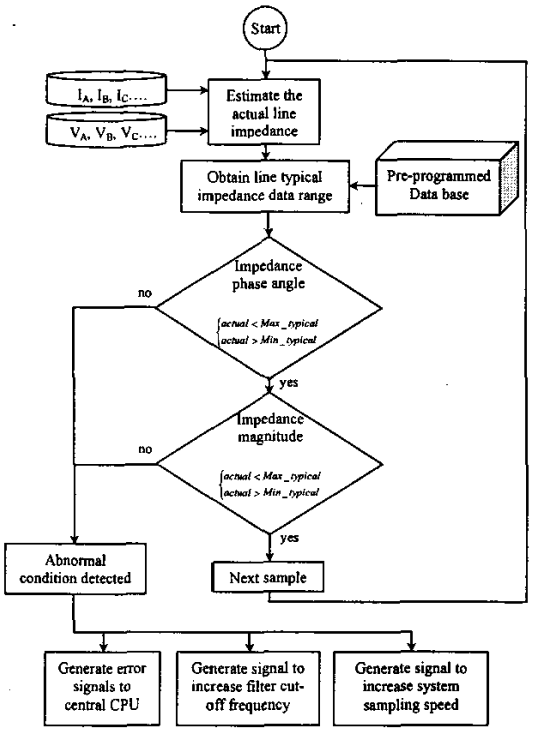

Figure 2. Flow chart of controller operation.

Achieving high speed with reduced complexity and size and minimal power dissipation is considered for the implementation of the intelligent controller. As observed from equation (5) and (6), the control algorithm for power system protection application contains square-root and arc-tan operations that are complex to realise in hardware and will significantly increase the controller delay, complexity, power consumption, and size. To overcome these issues, two approaches have been proposed.

Firstly, to eliminate the square-root operation, the square of the actual magnitude of the protected line impedance will be evaluated and compared to its typical value, instead of the line impedance magnitude. The typical value of the line impedance magnitude is stored in an electrically erasable programmable read-only memory (EEPROM), allowing users to re-program the impedance data when the relay is transferred to another line. When reading the impedance information from the EPPROM, the controller automatically takes the square of the impedance magnitude and compares it to the measured value.

Secondly, to eliminate the arc-tan function to reduce the cost of the control algorithm implementation, a novel approach to determine the phase angle of the protected transmission line is proposed as follows:

Recall from equation (5.1), let $v(t)$ and $i(t)$ be the instant line voltage and current seen from the relay, which can be expressed by [2]:

$$v(t) = V_P \sin(\omega t + \phi_v) = V_P \sin(\phi_1) \quad (7)$$

$$i(t) = I_P \sin(\omega t + \phi_i) = I_P \sin(\phi_2) \quad (8)$$

where $\phi_1 = \omega t + \phi_v$ and $\phi_2 = \omega t + \phi_i$ are the instant phase angles of the line voltage and current respectively.

Figure 5.8 illustrates the phasor diagram of the line voltage and current at the time instant t. It is observed that the purpose of equation (6) is to determine the phase angle of the protected line impedance (ϕ_{line}), which is the angle between the line current vector and the line voltage vector, as shown in Figure 5.8.

$$\phi_{line} = \arctan\left(\omega \times \frac{i(t)}{i'(t)}\right) - \arctan\left(\omega \times \frac{v(t)}{v'(t)}\right) = \phi_2 - \phi_1 \quad (9)$$

where $-90° \le \phi_{line} \le +90°$

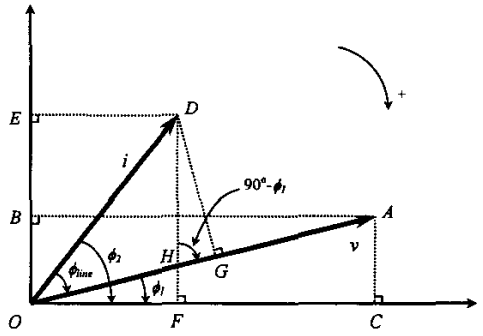

Figure 3. Phasor diagram of the line voltage and current.

Based on the phasor diagram and by considering similar triangles ΔOHF and ΔOAC, the right triangle ΔDGH and the right triangle ΔODG, sine of the line impedance angle can be determined using formula (10):

$$\sin(\phi_{line}) = \frac{GD}{OD} = \frac{i(t) \times v'(t) - i'(t) \times v(t)}{\omega \times V_P \times I_P} \quad (10)$$

However, equation (10) implies that a square-root operation will be required to determine the magnitudes of voltage and current. To eliminate the square-root operation when realising the control algorithm in hardware, the square of the sine of the line impedance angle will be used instead.

$$\sin^2(\phi_{line}) = \frac{\left[i(t) \times v'(t) - i'(t) \times v(t)\right]^2}{(\omega \times V_P \times I_P)^2} \quad (11)$$

$$\therefore \sin^2(\phi_{line}) = \frac{\left[i(t) \times v'(t) - i'(t) \times v(t)\right]^2 \times \omega^2}{\left[\left(v(t)^2 \times \omega^2 + v'(t)^2\right)\right]\left[\left(i(t)^2 \times \omega^2 + i'(t)^2\right)\right]} \quad (12)$$

The sign of impedance angle is determined by:

$$sign(\phi_{line}) = sign(\sin(\phi_{line})) = sign(i(t) \times v'(t) - i'(t) \times v(t)) \quad (13)$$

This proof will also be valid when $i(t)$ is lagging compared to $v(t)$, in which case will result in a negative

impedance phase angle. Moreover, this approach has been considered when $v(t)$ and $i(t)$ are located in other quadrants and proved to be valid.

In conclusion, to eliminate the arc-tan operation, the square of the sine of the impedance phase angle of the protected line impedance (with sign), instead of the impedance phase angle, will be evaluated and compared to the square of its typical value, which is stored in an EEPROM.

5. SIMULATION RESULTS

Three DAQ systems, employing a full flash ADC, a modified flash ADC and a modified flash ADC with reconfigurable property, have been designed and simulated. Figure 3 presents the plots of differential nonlinearity (DNL) and integral nonlinearity (INL) errors of the designed DAQ system employing modified flash ADC at a sampling frequency of 100MS/s. It can be seen that the DNL and INL achieved are 0.6 and 0.5 LSB respectively.

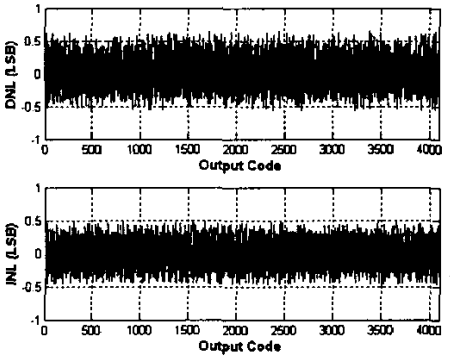

Figure 3. DNL and INL at 100MS/s.

The performance of the three approaches are summarised in Table 1. It is noted that the average power consumption and average data rate per channel of the system are when the reconfigurable architecture is applied.

From this analysis, we can conclude the advantages of the pipeline ADC employing a modified flash ADC architecture, which include, less components therefore smaller size, and lower power consumption. These characteristics make this new device better candidate for many applications where power and size are the major factors.

6. CONCLUSION

A reconfigurable DAQ architecture has been presented. The reconfigurable DAQ is employed in a digital relay for power system distance protection It can detect and adjust its sampling speed depending on the occurrence of a fault in the network.

Results indicate that a 33% power saving is obtained and 31% of die size could be saved when the new modified flash ADC is used instead of a full flash ADC. A further 87% reduction of power consumption is achieved, 98% average data throughput is obtained, and the total sampled data is reduced by 98% when the reconfigurable algorithm is applied. This significantly reduces the system need for data storage, and hence correspondingly reduces the system complexity, and also enables an increase of system detection speed and accuracy.

Table 1. Comparison results of the three DAQ architecture performance

	Using traditional flash ADC	Using modified flash ADC	Using modified flash ADC
Reconfigurable Property	*No*	*No*	*Yes*
Device delay			
Total delay	8ns	8ns	8ns
Max master clock speed	1GHz	1GHz	1GHz
Max data rate per channel	10MS/s	10MS/s	10MS/s
Average data rate per channel	10MS/s	10MS/s	204kS/s
Power consumption			
@ max sampling speed	97.2mW	64.9mW	64.9mW
Average Power consumption	97.2mW	64.9mW	8.4mW
Number of Devices			
PMOS	872	560	560
NMOS	911	626	626
Resistors	87	87	87
Capacitor	10	10	10
Other Parameters			
DNL	±0.5 LSB	+0.6/-0.5 LSB	+0.6/-0.5 LSB
INL	±0.5 LSB	±0.5 LSB	±0.5 LSB
Resolutions	12 bits	12 bits	12 bits
Supply Voltage	2.5V	2.5V	2.5V

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