Elemental diffusion at the GaAs/ZnSe interface

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Abstract- ZnSe epilayers were grown on GaAs using MBE. The native contamination (oxide and carbon) was removed from the substrate surfaces by conventional thermal cleaning and by exposure to atomic hydrogen. A maximum substrate temperature of 600°C was required for the thermal cleaning process, while a substrate temperature of 450°C was sufficient to clean the substrate using the hydrogen. ZnSe epilayers were also grown on As capped GaAs epilayers, which were decapped at a maximum temperature of 350°C. SIMS profiles confirmed that elemental interdiffusion across the interface is minimal for smooth substrates, which has been prepared by exposure to atomic hydrogen flux or using As capped GaAs buffer layer.

A. Introduction

The lack of high-quality ZnSe substrates has limited fabrication of most of the ZnSe based light emitting devices to nearly lattice-matched GaAs substrates or GaAs epilayer capped with arsenic. The lifetime of these devices has been increased from a few seconds [1] in 1993 to 9 hours [2] in 1995. In 1996, Sony reported a laser device with a lifetime of about 101 hours [3]. However, to commercialise these devices a lifetime of 10000 hours is necessary. Unfortunately, there has been no further improvement in the lifetime of these devices in the last few years. The quality and integrity of the ZnSe-based devices is dependent significantly upon the chemical and physical properties of the ZnSe/GaAs interface. In this paper, we report our investigation on the elemental interdiffusion across the ZnSe/GaAs interface, which may affect directly on the performance of the light emitting ZnSe-based devices.

B. Experimental Methods and Results

ZnSe epilayers were grown on GaAs (001) substrate using Molecular Beam Epitaxy (MBE). Substrates were degreased in 20 ml trichlorethylene for 120 s and then in 20 ml acetone for 60 s and finally in 10 ml methanol for 120 s in an ultrasonic bath. They were then rinsed with deionised water before being stirred in concentrated H2SO4 for 30 s to remove the excess water from substrate. Finally, the substrates were chemically etched in 20 ml of stagnant H2SO4/H2O2/H2O2 (6:1:1) volume ratio solution for 90 seconds while rapidly stirring to avoid selective etching or bubble formation on the substrates. The etch-rate is estimated to be about 1.5 μm/min [4].

The native contaminants (oxide and carbon) were removed in situ from the substrates surface by conventional thermal cleaning and by exposure to atomic hydrogen. A maximum substrate temperature of 600°C was required for the thermal cleaning process, while a substrate temperature of 450°C was sufficient to clean the substrate using the hydrogen cleaning process. ZnSe epilayers were also grown on As capped GaAs epilayers, which were...
decapped at a maximum temperature of ~ 400°C prior to the commencement of growth. The quality of the substrates was assessed using RHEED pattern. A streaky RHEED pattern before each growth run was indicating a clean and smooth substrate surface. In addition to the samples grown at La Trobe University (Australia), several samples from Würzburg University (Germany), which were grown in two different commercial MBE systems, have also been used in the current study. A similar sample preparation had been used prior to the growth process for the samples, which were acquired from the Würzburg University [5].

SIMS analysis was performed using a Cameca IMS-5f ion microscope at the Australian Nuclear Science and Technology Organization (ANSTO). Positive secondary ions CsO+ were detected to provide a depth profile using a 15 nA primary Cs+ ion current at 3 keV impact energy, rastered over a 250 × 250 μm area. The ion count rate was normalized to Cs+ secondary ion counts rate to minimize the effect of variations in the primary ion beam current. The experimental conditions for SIMS analysis are given in [6]. The raw data was converted to the quantitative data using the estimated “useful ion yield” of Ga and As in ZnSe-matrix and Zn and Se in GaAs-matrix obtained by depth profiling of ion implanted standard samples.

The interface widths of epilayers with different thickness were examined and it is found that there is no correlation between the ZnSe epilayer thickness (growth time) and the interface width. Table 1 summarises the slope of the trailing edge (TE) of Zn profile of some selected samples with different thickness, and different substrate preparations. Here, the width of the TE of Zn has been taken as a criterion for diffusion length. ZnSe samples LTU#38, LTU#41, and LTU#42 were grown on As capped GaAs epilayers with different thickness. An increasing in the TE of Zn of 5 nm has been observed for the sample with 330 nm compare to 2 nm thick layers. This variation does not suggest that growth time significantly increases Zn diffusion into GaAs substrate, since 5 nm is within the depth resolution of SIMS analysis.

This study has also shown that different preparation methods; the hydrogen cleaning, the As-capped GaAs epilayer, and the conventional thermal cleaning have little or no effect on the elemental interdiffusion across the ZnSe/GaAs interface, if the substrate surface is relatively smooth. The TE of Zn at ZnSe/GaAs interface varies by few nm (less than 10 nm) for the substrates, which have been prepared using different methods, see table 1.

Table 1: The slope of TE of Zn profile measured from some selected samples with different thickness giving the substrate preparation used.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Substrate</th>
<th>Thickness [nm]</th>
<th>TE of Zn [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTU#5</td>
<td>Thermal cleaning</td>
<td>540</td>
<td>20</td>
</tr>
<tr>
<td>LTU#38</td>
<td>Epilayer</td>
<td>330</td>
<td>17</td>
</tr>
<tr>
<td>LTU#41</td>
<td>Epilayer</td>
<td>80</td>
<td>13</td>
</tr>
<tr>
<td>LTU#42</td>
<td>Epilayer</td>
<td>2</td>
<td>12</td>
</tr>
<tr>
<td>LTU#48</td>
<td>Hydrogen cleaning</td>
<td>1130</td>
<td>14</td>
</tr>
</tbody>
</table>

ZnSe Samples listed in table 1 have been grown on a smooth GaAs surface, (confirmed by streaky RHEED pattern observations). The preparation method of the substrates does not have a distinguishable effect on diffusion length. However, the conventional thermal cleaning could enhance the elemental interdiffusion across the interface, if the cleaning process produces a rough substrate surface, see figure 1. In fact, this may often
happen for the thermal cleaning process of GaAs substrate, due to lack of As over pressure in II-VI MBE chamber. This may consequently cause As desorption from substrate during the native oxide desorption process, and produce a rough surface.

Figure 1 (A) and (B) show depth profiles of ZnSe/GaAs interface of a hydrogen-cleaned substrate and a thermally cleaned substrate, respectively. Here, the thermal cleaning process has roughened the substrate; it can be seen that the interface is much broader than that of the hydrogen cleaned substrate.

The slope of the LE edge of Ga and As, and the slope of the TE edge of Se and Zn, and the FWHM of the GaSe peak at the interface have been measured for these samples, and are listed in table 2. The slope of the LE edge of Ga and As has been increased by a factor of ~ 10 and ~ 17, respectively, and the slope of TE edge of Se, and Zn, and the FWHM of GaSe peak has been increased by a factor of ~ 20 for the thermally cleaned sample. This indicates that a rough surface of GaAs substrate will radically enhance the elemental interdiffusion process across the interface. This implies that the most reliable preparation methods for GaAs substrates are the hydrogen cleaning and As-capped epilayers.

Fig 1: Depth profile of ZnSe/GaAs interface of a hydrogen-cleaned substrate (a), and depth profile of ZnSe/GaAs interface of thermally cleaned substrate (b).
Table 2: The slope of the LE and the TE of the elements across the ZnSe/GaAs interface, and the FWHM of GaSe peak for a hydrogen-cleaned substrate and a thermally cleaned substrate, which produced a rough substrate surface.

<table>
<thead>
<tr>
<th></th>
<th>Smooth substrate (Hydrogen Cleaned)</th>
<th>Rough substrate (Conventional Thermal clean)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ga (LE)</td>
<td>17 nm</td>
<td>175 nm</td>
</tr>
<tr>
<td>As (LE)</td>
<td>10 nm</td>
<td>167 nm</td>
</tr>
<tr>
<td>Zn (TE)</td>
<td>8 nm</td>
<td>170 nm</td>
</tr>
<tr>
<td>Se (TE)</td>
<td>9 nm</td>
<td>165 nm</td>
</tr>
<tr>
<td>GaSe (FWHM)</td>
<td>10 nm</td>
<td>200 nm</td>
</tr>
</tbody>
</table>

C. Conclusion

A small dependency between the interface thickness and the ZnSe epilayer thickness has been observed. Evidences have been presented for the effect of the substrate surface quality on the elemental interdiffusion across the interface. A minimum of ~ 20 nm thick interface has been observed for a smooth GaAs surface, which has been cleaned by atomic hydrogen flux, while a ~ 200 nm thick interface has been observed for a rough substrate surface, which has been prepared by the conventional thermal cleaning. It has been observed that the thermal cleaning of the GaAs substrate may often roughen the surface and enhance the elemental interdiffusion across the interface. This study showed that a smooth and with the highest quality substrate can be achieved by exposure to atomic hydrogen flux or using As capped GaAs buffer layer.

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References