Investigation Of Multirate Techniques For Digital Generation Of Transmitter Signals For TIGER Radar

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I Introduction

Ionized gases from the sun disturb the interplanetary space and earth's magnetic field that has significant impact on our technological lifestyle including disruption of communications system, changes in satellite orbits and failure of satellite system due to collision of energetic particles. This ionized gas or plasma is generated from Sun at typical speed ranging from 400 to 800 Km per second and known as solar wind [1]. Our Earth is protected from the solar wind by its magnetic field called magnetosphere.
The thickness of the magnetosphere is approximately 70,000 km towards Sun and around 1000,000 Km in antisunward direction [5]. At high altitudes transferred solar energies are higher and are low at lower boundaries of the magnetosphere. The lower boundaries called ionosphere that meets with upper atmosphere of the Earth around altitudes of 100,000 Km [5].
The solar wind or interplanetary magnetic field transfers some form of energy to Earth's magnetic field. This process distorts the magnetosphere and generates large scale electric and magnetic field that energize magnetospheric plasma populations. The solar energy is transferred to ionosphere because of the interconnection between magnetosphere and ionosphere. The energetic particles from the solar wind are responsible for aurora, emitted light from collision of incoming particles with atmospheric atoms and molecules. The disturbances caused by solar wind are imaged in the ionosphere at high altitudes. Therefore ionosphere can be used as viewing screen on which we can globally observe the space weather disturbances in the magnetosphere.

SuperDARN (Super Dual Auroral Radar Network) is an international radar network, which evaluates the space weather system. Tasman International Geospace environment radar (TIGER) is one component of the SuperDARN network that analyzes the space weather in southern hemisphere. This radar started its operation in December 1999 and successfully analyzing ionospheric irregularities. The operating frequency and beam selection procedure of the transmitter are controlled with computer through Internet. The transmitting pulses are modulated using analog heterodyne operations and each of 16 transmitter antennas is fed by a separate power transmitter module. The analog transmitter system is discussed in detail in section III.

In this paper we present a digital counterpart of current analog transmitter system. In section II modulation schemes are described for past and present communication systems. Section III gives the overview of current analog model and in the following section the proposed digital system is discussed. The baseband signal is upconverted using FIR filter and simulation results are given in section IV. Polyphase filters are recently proved to be very efficient for communication systems largely because of two factors. These are discussed in section V. The digital equivalent of beam steering part of the analog system is presented in section VI. Reconfigurable devices are heart of the hardware for digital system and are discussed in section VII. The proposed digital modulator is implemented as a prototype on Altera FPGA its basic blocks are discussed in section VIII. In last section conclusions are drawn.

II Traditional Modulation Schemes in Signal Generation

In conventional transmitters a balanced mixer and analog filters are used for frequency translation or channelization. The frequency resolution of the analog synthesizer depends on the required application. The analog components introduce distortion in the signal and these effects are related to non-uniform gain and phase of analog filters and imbalance in the modulation process. The nonlinearities caused by the analog systems also include DC offset, intermodulation terms from mixing processes and non-linear amplitude responses of different circuit elements [6]. These distortions can mostly be mitigated using Digital Signal Processing (DSP) techniques.

In first generation communication systems a Digital to Analog Converter (DAC) is placed before mixing. The analog mixers and analog filters create distortion in the signal. These effects may be temperature and time dependent therefore they are not completely eliminated with analog filtering and conditioning. Some of these distortions can be reduced with DSP techniques which can be applied on reduced sampling rate.

Second generation transmitters put the DAC after mixer, the mixing operation is then performed in the digital domain which reduces the distortion resulting from analog components. Intermodulation terms and mismatching problems can easily be handled using DSP techniques. Mixing in digital domain also eliminate the DC injection problem. The disadvantage of this class is large
computations which are involved in processing the sine or cosine multiplication. In third generation transmitters, intentional aliasing is used for IF translation. This class of modulator does not need any mixing, a Direct Digital Synthesizer (DDS) or a sine or cosine generator. Multirate processing is used to obtain heterodyne operation in digital domain. Our proposed digital modulator is in this third generation class and is discussed in section IV.

III Current Analog architecture of TIGER transmitter

The TIGER radar is installed in Bruny Island, Tasmania and it covers the auroral and sub-auroral ionospheres South of Australia. The radar detects ionospheric scatter and determines the echo power, Doppler spectrum, as well as the azimuth and elevation angles of arrival. The TIGER transmitter is set of 16 transmitters connected with a single log-periodic antenna and frequency range varies from 8MHz to 20MHz. This operating frequency enables the transmitted vector to achieve oblique incidence in the ionosphere and reflect back to the radar receiver [2]. Each beam is transmitted at 600W and is directed through a phasing matrix with constant delay or phase. The block diagram of the TIGER radar is shown in Figure 1, which outlines mainly the transmitter section.

![Figure 1. Simplified block diagram of SuperDARN Radar](image)

The analog frequency synthesizer has main role in selecting the operational frequency for the transmitter beam. The mixing operation is performed using a local oscillator with frequency range of 48-60 MHz and multiplied with a reference input of 40.625 MHz. A bandpass filter is used to suppress frequencies out of 8-20 MHz bandwidth. The timing pulses are controlled by a computer through modem, which are normally not continuous. A regular pulse train for the radar is not suitable because of Doppler shift in the echoes; therefore pulse train with varying time slots is modulated. The typical pulse length is 300usec for 45Km range resolution and radar uses a number of different multipulse transmission sequences consisting of typically 13 pulses over a100ms time [5]. The transmitted beams are centered at intervals of approximately 3.6 degrees and 16 beams give azimuth sweep of approximately 50 degrees. The phasing matrix is implemented as variable time delay shown in Figure 1. For each beam the time delay is fixed, which means phase delay is varying with frequency. The azimuth beam width decreases with increase in frequency [5].

IV Proposed Digital Transmitter system

In the literature different methods described for achieving RF modulation. Most of these techniques use some type of sine or cosine multiplication that involves power sensitive signal processing function. Using multirate digital techniques this can be implemented as a simple logic. In this section we present an equivalent method of generating digital signals for existing analog TIGER transmitter. We propose digital equivalent of only beam generation system of the transmitter while power amplifier and other associated analog circuitry remain the same. The block diagram of the proposed method is shown in Fig. 2. The input Gaussian pulse is resampled at higher clock rate and a high pass FIR filter is applied to generate the high frequency transmission signal. The process of upsampling and filtering can be combine in one block as a polyphase filter [4]. The time delay is introduced to steer the beam at a set azimuth angle. This digital signal is converted to the analog domain using a suitable DAC and a suitable analog reconstruction filter (ARF) is applied to reduce the quantization noise. The output of ARF is sent to the existing power amplifier through transmitter/receiver switch.

The frequency range of input pulses varies between 200KHz to 500KHz and this 'baseband' signal is shifted to bandwidth of 8MHz to 20MHz by the upsampling process. The upsampling process introduces L-1 spectral copies in the signal spectrum when the signal is upsampled by a factor of L. FIR filtering is used to select desired spectral copy and suppress other images. FIR digital filters are linear phase filters with very narrow transition band. The symmetric and linear properties of FIR filter make it attractive for communication systems [3]. As described in the previous section TIGER radar transmits a selected beam from the azimuthal range of approximately 50 degrees. To introduce an approximate phase delay in each beam a different constant time delay is inserted in each modulated pulse.

Simulations have been carried out to generate modulated Gaussian functions at RF frequencies of between 8MHz
Figure 2. Block diagram of proposed digital transmitter

and 20MHz. The baseband pulses are selected at frequency range of 200KHz to 500KHz, the frequency spectrum of the generated Gaussian envelope is shown in Fig 3 (a). The baseband signal is upsampled to sampling frequency of 20MHz with Nyquest frequency of 10MHz. This signal is filtered by 200 tap high pass FIR filter with a cutoff frequency in this example of 10MHz. The frequency response is shown in Fig 3 (b). The FIR filter was designed using Kaiser_Bessel window with parameter 10.

Figure 3 Spectrum of Gaussian pulse and FIR filter with cutoff frequency at 10MHz.

The FIR high pass filter removes all other spectral copies of the spectrum except at the Nyquest frequency. The maximum sampling rate can be 40MHz for 20MHz transmission signal and to avoid distortions in ARF the input sample rate should not be less than ten times the sampling of the modulated pulse.

The output envelope and frequency response of filtered Gaussian pulse is shown in Figure 4. The nominal width of the modulated pulse is set to 300 usec that can cover 45 km range for the TIGER transmitter. The spectrum of the simulated signal clearly indicates the modulated pulse at 10MHz and shows it has no unwanted images.

Figure 4 Signal envelope (b) the frequency response of transmitted signal

V Polyphase implementation of FIR Filters

Polyphase filters are being increasingly used largely due to their efficient use of resources when implemented in hardware. Fig 5 illustrates the working principle of a polyphase filter. The filter impulse response of an N tap FIR can be divided into L sub-filters, where L is upsampling factor. We have considered the previous example of 200 tap FIR filter that operated on resampled Gaussian pulse. The FIR filter response is now decimated to a polyphase network of forty sub-filters each contains five taps. Each branch of the polyphase filter contributes to one nonzero sample at the output, which is one of 40th of
the newly upsampled signal. The advantage of polyphase filter is that it performs filtering at low sampling rate [7]. The filter coefficients of polyphase filter can be written as 

\[ h_p[n] = h[nL + p] \]

Where \( h_p[n] \) are polyphase filter coefficients and \( L \) is upsampling factor. As can be seen from Figure 5 for each new input sample there are forty output samples.

![Figure 5 Block diagram of 200 tap polyphase filter.](image)

VI Phasing Matrix using variable time delay

TIGER transmitter modulates each beam in certain azimuth angle as described before. The phase angle can be implemented using variable phase or constant time delay. In analog circuitry this has been performed with varying the time delay for each beam and therefore the frequency would be changed in proportion to phase change. In proposed method variable time delay is inserted in each modulated pulse. The results have been acquired with simulations of three channels with time delay equivalent of phase of four degrees in each channel as depicted in Fig. 7. The simualted result shows larger picture of the signal envelope when the sampling window is placed around the peak amplitude with window size of 150 samples. The peak of signal envelope in the sampling window moves with the time delay. The diagram shows the change in the amplitude and phase angle with a constant time delay for each signal beam. In these results positive angles are assumed and this can also be simulated as negative time delay. In this case transmitted beam can either be switched to right or left depending on the time delay.

![Figure 7 The output of phasing matrix for three channels with time delay.](image)

The proposed method can generate the TIGER frequency range with varying the resampling rate and changing the filter coefficients. To avoid the aliasing problem the sampling frequency must obey the Nyquist criterion. The method is suitable for devices with fast sampling clock and for application circuits which can change the configuration on the fly.

VII Reconfigurable Devices

FPGA’s are reconfigurable devices that provide excellent hardware solution for our system. They are relatively fast devices and system can be designed with parallel processing paths to meet the processing speed.
requirements. The processing can be tailored for different system operating modes with the help of reconfiguration property. Reconfigureable devices provide high efficiency since system can be implemented in parallel form at functional unit level. The functional unit contains small cells of memory, which can be accessed in a single clock cycle. Therefore memory bandwidth and throughput rate is much higher than traditional DSP chips [8]. A potential application of FPGA is time shared implementation or dynamic reconfiguration of hardware. In this application a portion of FPGA is reconfigured on the fly when it is performing signal processing task. For example an FPGA based system can work as a digital transmitter and a receiver at different times [12].

VII.I Structure of Altera FPGA

Proposed method is emulated on Altera FPGA and now we present some basic building blocks of this device. The Flex10k20 has three level of hierarchy as in normal FPGA with lowest level contains lookup tables (LUT) in the form of logic element (LE). Each LE contains a four input LUT, a flip flop and special carry circuitry for arithmetic operations [13]. Flex10k20 comes with 1,152 LE and 20,000 gates. Each logic array block (LAB) comprises 8 LE and there are 144 LAB in Flex10k20 [13]. The device also has unique hardware part called Embedded Array Blocks (EAB). These blocks can be designed as variable size of RAM to implement complex logic circuit such as multiplier.

VII.II System Design with VHDL

To design digital systems on FPGA a hardware language is used called VHDL, which stands for VHSIC Hardware Description Language (HDL). The term VHSIC means Very High Speed Integrated Circuits such as FPGA. VHDL represents two type of circuit approximation one is structural and second is behavioural description [9]. In structural form the integrated circuit is described with detail of structure and interconnections. The second type represents the algorithmic form of the system, which normally is not optimized in the sense of speed and silicon area. However it permits the designer to test the system prototype without much knowledge of the structure. The design cycle for testing a prototype system include defining the algorithm in VHDL, test the logic with VHDL compiler, prepare the logic to load into FPGA hardware and the last step is to debug the system and change the logic in VHDL editor if required.

VIII FIR filter implementation

The FIR filter implementation onto FPGA hardware requires the knowledge of number of filter characteristics. The performance of the filter is mainly based on the filter coefficients, input data and the length of the filter. Another important characteristic for measuring the filter efficiency is sampling rate that determines the cutoff frequency. There are number of techniques to implement FIR filter with varying performance and hardware utilization. We briefly discuss two cases with consideration of speed and hardware utilization.

VIII.I Parallel Method

In this method the filter operates in parallel form with an N tap filter requiring N multipliers and N-1 adders. For the case of a five tap FIR filter shown in the Figure 8, five multiplier and four adders are used. The Gaussian samples and scaled arithmetic filter coefficients of filter are stored in a LUT, for simplicity these are not shown in the diagram. In this method, output samples are available after one clock cycle ignoring the propagation delay and settling time of the registers. The filter throughput is very high and does not depend on the filter length. Parallel architecture is very fast but with a disadvantage of using more precious silicon area. Hardware area grows linearly with an increase in the number of filter taps [10].

Figure 8 Parallel architecture for FIR filter

VIII.II Sequential Method

In the parallel implementation of the FIR filter the multiplier and adder circuits require the most silicon area. By resource sharing and time-multiplexing our signals the FIR filter can be implemented using a single multiplier and adder. While this does produce a significant reduction in the use of silicon, it comes at the cost of additional control circuitry registers and increased delay. As hardware efficiency was a major factor in the construction of the prototype this method was chosen for the implementation of the FIR filter. For the prototype of the digital transmitter we used a FIR filter of five taps. The basic building blocks are shown in Figure 9. The filter coefficients and the input Gaussian samples are quantized and stored in LUT as 9bits 2's compliment numbers. Since the input samples are positive and negative the signed multiplier is required. The control logic generates handshaking signal to synchronize the operations of mux, multiplier, adder and accumulator. The filter response of the filter is convolved with input Gaussian samples. To achieve convolution in a serial implementation the data samples are delayed and multiplied with each filter coefficient in turn.
The quantization of filter coefficients and data samples introduce non-linear distortion of the signal. The signal to noise ratio (SNR) can be increased by increasing the number of bits for the data samples and filter coefficients. For an increase of one bit, the dynamic range is increased by 6dB [8].

![Diagram of sequential implementation of FIR filter]

Figure 9 Sequential implementation of FIR filter

The prototype has been implemented using Visual HDL, a graphical design package from Innoveda and VHDL. A block diagram for the control logic is shown in Figure 10. The control block generates control signals for accumulator register and multiplexers, to ensure the orderly transfer of samples to multiplier and adder. It also creates an accumulator clock signal that operates slower than the input clock to allow for propagation delay through the multiplier and adder. After an output sample has been generated the accumulator is cleared so that calculation of the next output can commence using the next five samples of the input data.

![Diagram of control logic in VHDL]

Figure 10 Control logic in VHDL

A prototype Gaussian modulator, consisting of Gaussian pulse generator and FIR filter has been implemented on an Altera Device Flex10k20 using MaxPlus II compiler and programmer tools. Output from the prototype Gaussian modulator is shown in Figure 11, as displayed on a digital cathode ray oscilloscope (CRO). The approximate number of 15000 gates has been used in the implementation. As silicon space efficiency is an important issue in our design criterion, future research will be to investigate more advanced techniques to reduce the design area. One of the efficient methods is distributed arithmetic which does not depend on filter length [11]. Another possible solution for less hardware utilization is multiplierless model. In this case filter coefficients are required to be in two's power form [8].

![Diagram of output envelope of the modulated signal]

Figure 11 Output envelope of the modulated signal.

IX Conclusions

Research has been carried out on possible methods for the digital generation of signals for the TIGER transmitter. The simulation results have shown that the polyphase network provide better performance compared to FIR filter. The lower sampling rate of polyphase filters make it a good candidate for applications with high throughput requirement. Implementation of FIR filter is addressed with a technique which is less sensitive to hardware utilization. A hardware prototype has been constructed using an Altera Flex 10k20 device. Results demonstrate the feasibility of using FPGA devices for the complete implementation of a digital TIGER transmitter.
X References